NASA CR-
147416

TECHNICAL DESCRIPTION OF A TAPE CONTROL UNIT FOR A HONEYWELL DDP-516 MINICOMPUTER

Job Order 35-489

Prepared By

Lockheed Electronics Company, Inc.
Aerospace Systems Division
Houston, Texas

Contract NAS 9-12200

For

CONTROL SYSTEMS DEVELOPMENT DIVISION

National Aeronautics and Space Administration

LYNDON B. JOHNSON SPACE CENTER

Houston, Texas

October 1975

LEC-6477

TECHNICAL DESCRIPTION OF A TAPE CONTROL UNIT FOR A HONEYWELL DDP-516 MINICOMPUTER

Job Order 35-489

PREPARED BY

J. C. Bergmann, Senior Engineer

APPROVED BY

Swan D. Person
Job Order Manager

Marion W. Schellhase
Associate Operations Manager

Prepared By

Lockheed Electronics Company, Inc.

For

Control Systems Development Division

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
LYNDON B. JOHNSON SPACE CENTER
HOUSTON, TEXAS

October 1975

LEC-6477

TECHNICAL REPORT INDEX/ABSTRACT

(See instructions on reverse side.)

1. TITLE AND SUBTITLE OF DOCUMENT

Technical Description of a Tape Control Unit for a Honeywell DDP-516 Minicomputer

2. JSC NO.

JSC-10651

3. CONTRACTOR/ORGANIZATION NAME Lockheed Electronics Company, Inc.	4. CONTRACT OR GRANT NO. NAS 9-12200
5. CONTRACTOR/ORIGINATOR DOCUMENT NO. LEC-6477	6. PUBLICATION DATE (THIS ISSUE) October 1975
7. SECURITY CLASSIFICATION Unclassified	8. OPR (OFFICE OF PRIMARY RESPONSIBILITY) W. L. Swingle
9. LIMITATIONS GOVERNMENT HAS UNLIMITED RIGHTS [X] YES [ ] NO IF NO, STATE LIMITATIONS AND AUTHORITY	10. AUTHOR(S) J. C. Bergmann
11. DOCUMENT CONTRACT REFERENCES	12. HARDWARE CONFIGURATION
WORK BREAKDOWN STRUCTURE NO. N/A	SYSTEM N/A
CONTRACT EXHIBIT NO. N/A	SUBSYSTEM N/A
DRL NO. AND REVISION N/A	MAJOR EQUIPMENT GROUP N/A
DRL LINE ITEM NO. N/A	

13 ABSTRACT

Detailed description of a digital magnetic tape control unit which interfaces up to four Ampex seven-track, magnetic tape transports to a Honeywell DDP-516 Minicomputer.

14. SUBJECT TERMS

Interface	Minicomputer-Interface	
Minicomputer	Magnetic Tape	
Mass Storage	Magnetic Tape Control Unit	

FOREWORD

This report describes the detailed operations and programming requirements of a Tape Control Unit built by the Lockheed Electronics Company Flight Controls Section. This Tape Control Unit is used to interface Ampex Magnetic Tape Transports to a Honeywell DDP-516 Minicomputer. The Tape Control Unit, DDP-516, and other peripheral devices form a major portion of the Flight Controls Laboratory and is used during Shuttle Flight Control Subsystem testing.

CONTENTS

TABLES

FIGURES

ACRONYMS

BCD	Binary Coded Decimal
CPU	Central Processor Unit
DMC	Direct Multiplex Control
FCL	Flight Controls Laboratory
I/O	Input/Output
JSC	Lyndon B. Johnson Space Center
LEC	Lockheed Electronics Company
MTT	Magnetic Tape Transport
NRZ	Nonreturn-to-zero
OCP	Output Control Pulse
SMK	Set Mask
TCU	Tape Control Unit

1. INTRODUCTION

The Tape Control Unit (TCU) described by this report was built by the Lockheed Electronics Co. (LEC) Flight Controls Section in response to operational requirements of the Flight Controls Laboratory (FCL). This TCU was designed to interface up to four Ampex Magnetic Tape Transports to a Honeywell DDP-516 Minicomputer.

This TCU is a copy of an existing unit which was built previously by the Flight Controls Section. The two tape control units are identical except for the computer input/output (I/O) address and the Direct Multiplex Control (DMC) channel assignment. The DDP-516, the two tape control units, their associated tape transports, and other peripheral devices are located in room 1047 of Building 16A, at the Johnson Space Center (JSC) and are used to support Shuttle Flight Control Subsystem testing. The primary use of the TCU's is for program storage, Fortran library storage, object code storage during assembly or complier operations, and for utility program storage.

This report is a detailed description of the operation of the TCU and is intended to be used as an instruction or troubleshooting manual for both TCU's.

2. DESCRIPTION OF TAPE CONTROL UNIT

2.1 TAPE FORMATS

Data are recorded on the magnetic tape in a nonreturn-to-zero (NRZ) mode, that is, each time the datum is a binary 1 a flux reversal is written on the tape. No flux reversal is made for a binary zero. Data are written on the tape as 7 lateral bits one of which is always a parity bit and, thus, not part of the original data word. Each group of 7 bits (6 data plus 1 parity) makes up one character. A character has no temporal distribution between bits but it has spatial distribution along the lateral axis of the tape. Each computer word consists of 12 or 16 bits and therefore requires either two or three characters to store it on the magnetic tape.

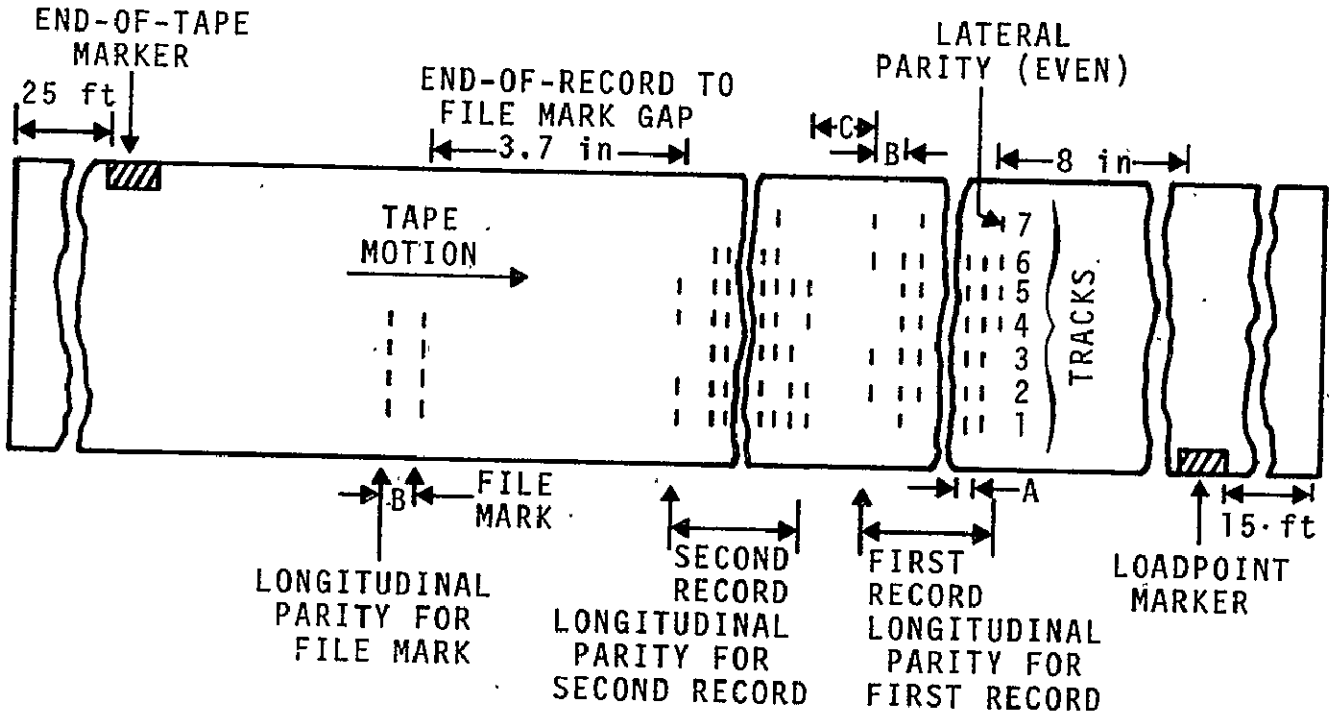
Data are stored on the tape in the form of records whose lengths are variable depending on the number of characters per computer word (two or three) and the total number of computer words to be stored on the tape. Each record has (on the end of it) a longitudinal parity character which is separated from the main record by four blank character spaces. (See figure 2-1.)

A file mark can be written on the tape to index a record or group of records. It consists of a one-character record with the data value of octal 17_8. A longitudinal parity bit is also written. Because longitudinal parity is even parity, the longitudinal parity character is also an octal 17_8. The file mark is the only single character record that can be written on the tape.

2.2 BLOCK DIAGRAM OPERATION

The TCU consists of eight major blocks as shown in figure 2-2. These major functional blocks are listed below:

- Address and control
- Motion control
- Read logic



NOTES: A — CHARACTER SPACING

200 BPI = 0.005 in
556 BPI = 0.001 in
800 BPI = 0.0012 in

B — NO-DATA GAP

200 BPI = 0.0207 in
556 BPI = 0.0075 in
800 BPI = 0.0054 in

C — INTER RECORD GAP, 3/4 in

Figure 2-1. — Tape format.

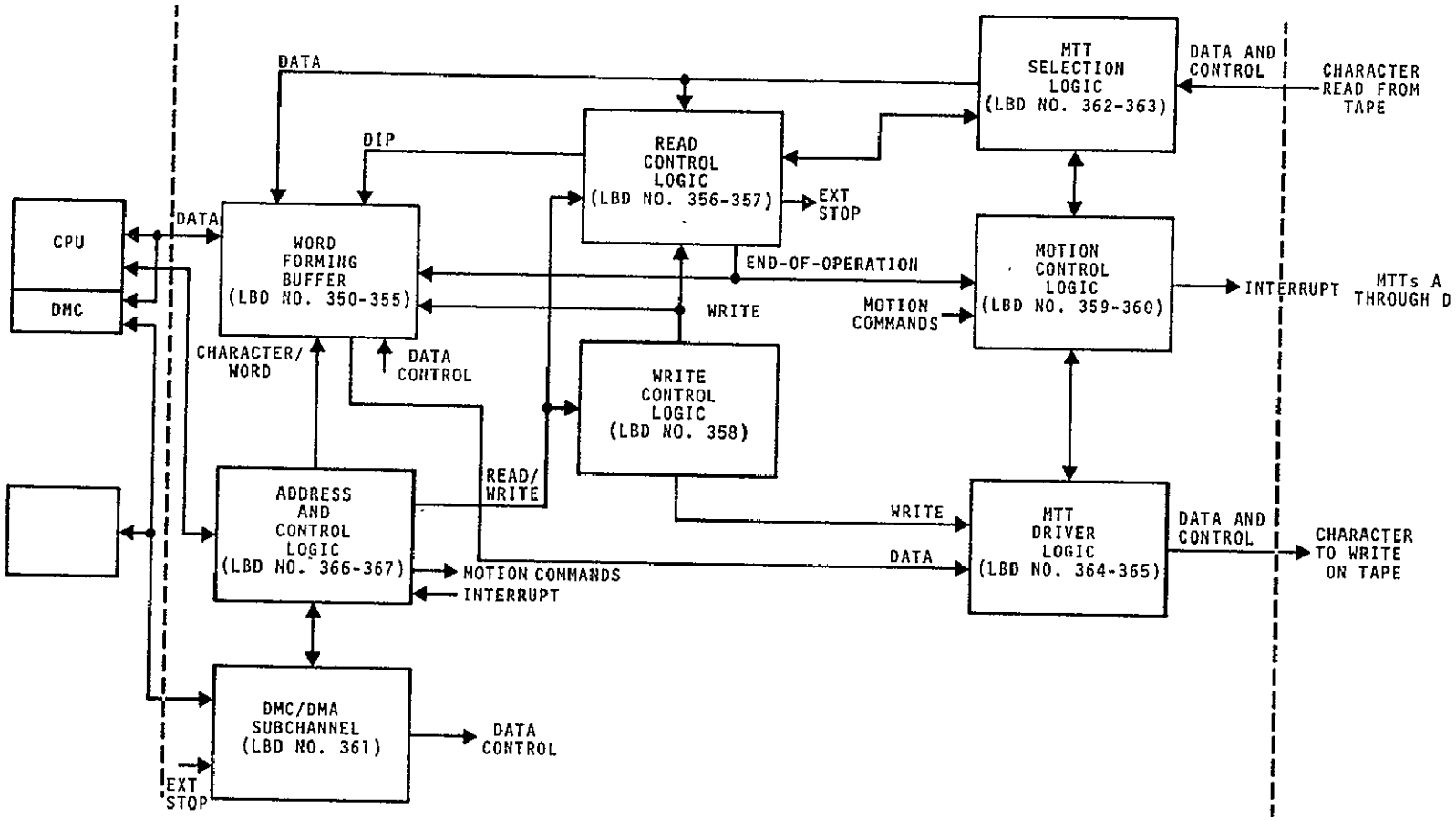


Figure 2-2. — Block diagram.

- Write logic
- Magnetic Tape Transport (MTT) selection logic
- MTT drivers
- Word-forming buffer
- DMC subchannel

The address and control logic accepts command and address words from the Central Processor Unit (CPU) and converts them into TCU commands which initiate the desired response. It also generates the necessary handshake signals which are sent back to the CPU.

The motion control logic controls the direction and start-stop times of the selected MTT. The motion control of the selected MTT is implemented by a set of forward, reverse, and rewind flip-flops. The correct motion delays in forward and reverse operations are generated in the motion control logic.

The read logic checks the lateral parity of the data read from the MTT. It also contains the end-of-record gap detection circuit, file mark detection circuit, and the read strobe generator.

The write logic contains the high-low density clock and the frame rate clock circuits. The write oscillator delay signal along with the write strobe pulses are generated in the write logic. It also contains the logic which establishes the load point gap, record gap, and the file gap.

Magnetic Tape Transport selection logic generates the MTT select signals and acts as the input buffer between the MTT and the TCU for data and control signals.

MTT driver logic contains the data and control signal drivers which serve as the output buffers between the TCU and the selected MTT.

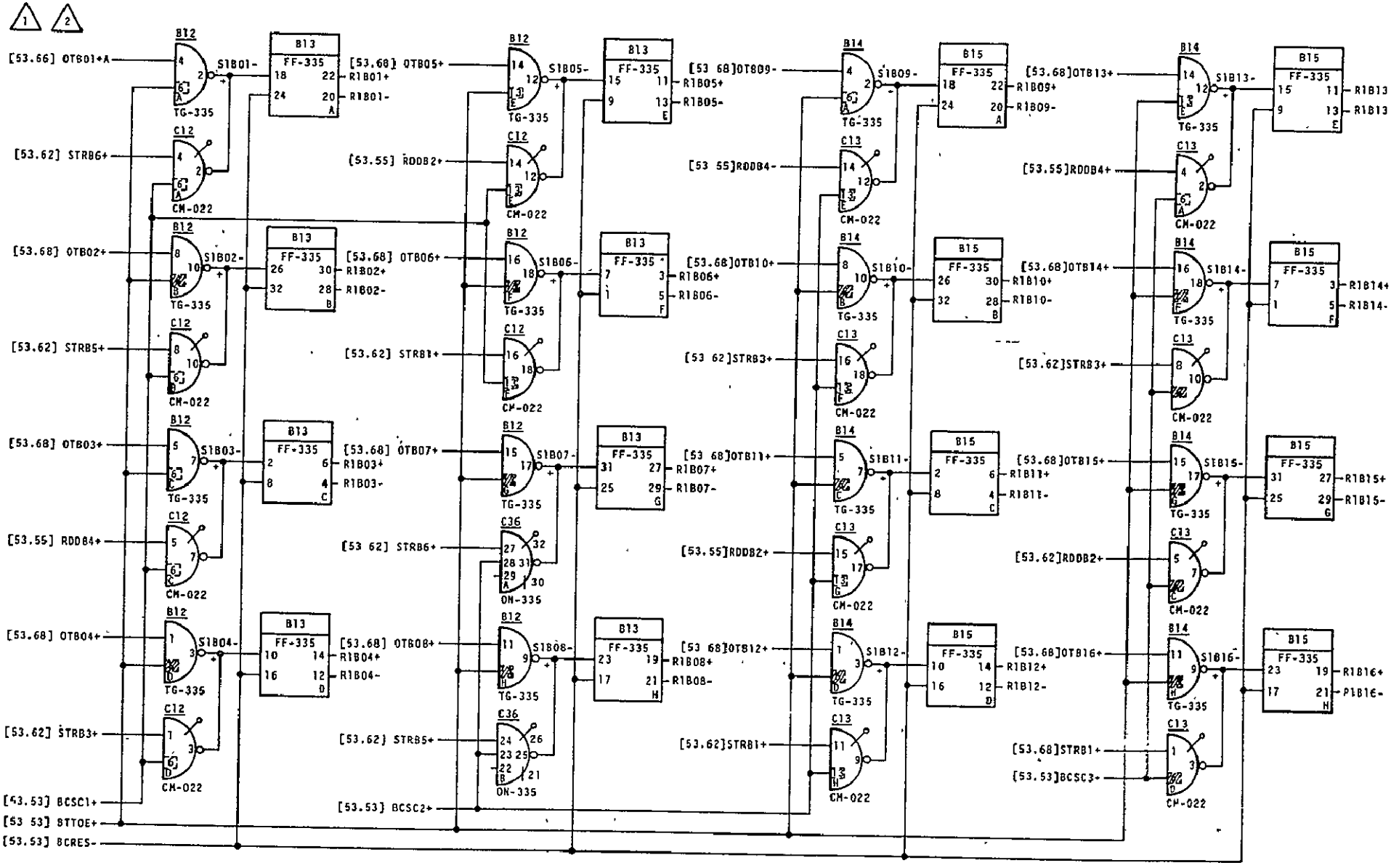


Figure 2-3. – Input buffer.

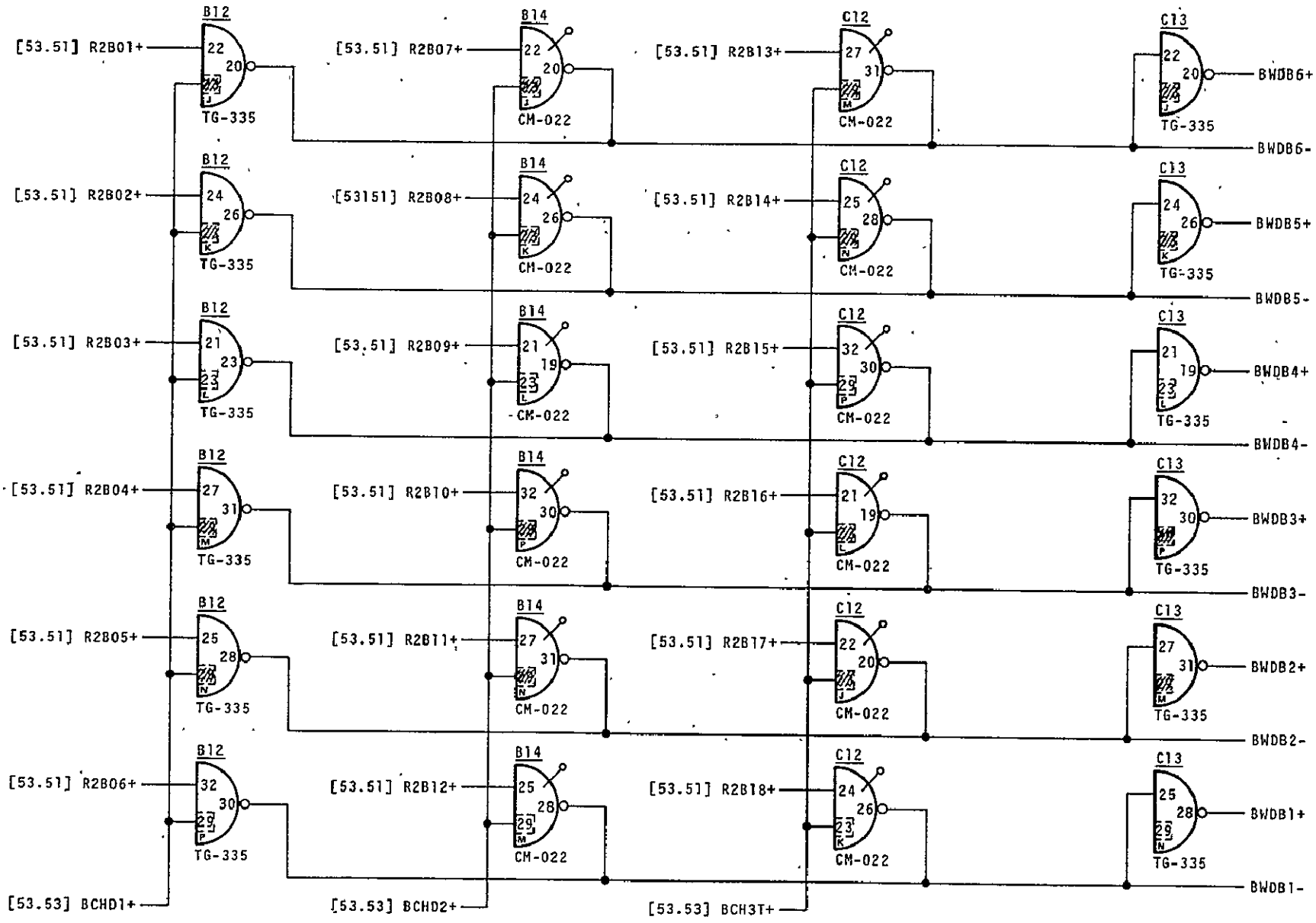


Figure 2-4. — Output buffer.

The word-forming buffer contains a double-rank buffer (two 16-bit registers) which provides one-word time for the CPU to acknowledge a data request. The word-forming buffer also contains the necessary control for processing and converting 6-bit tape characters into 16-bit computer words (figures 2-3 and 2-4).

The DMC subchannel permits the TCU to communicate with the CPU via the DMC option for more efficient data handling.

2.3 DETAILED DESCRIPTION

2.3.1 WORD-FORMING BUFFER LOGIC

The word-forming buffer consists of two 16-bit buffer registers which allow the CPU to receive or transmitt one complete 16-bit word at a time (figure 2-8). There is also the necessary logic to reform the 16-bit computer word into two or three 6-bit characters for the MTT (figure 2-4). It also has the logic to recombine the 6-bit characters from the MTT into 16-bit computer words. The lateral parity bit and the longitudinal parity character are also formed here.

The first 16-bit buffer register is the input buffer and it accepts computer words from the input bus in a 16-bit parallel format. It also accepts the data from the MTT but it is accepted in a 6-bit character sequential format. Thus this buffer acts as the data input device to the TCU.

The second 16-bit buffer register receives its data parallel mode from the input buffer. This is the TCU data output buffer and either transmits its data in 6-bit bytes plus one lateral parity bit to the MTT drivers or to the CPU via the input bus in 16-bit bytes. Before the data is transmitted to the MTT it is formatted by the buffer control logic (figure 2-5).

The buffer control logic contains the necessary logic to break up the 16-bit word stored in the output buffer into 6-bit bytes.

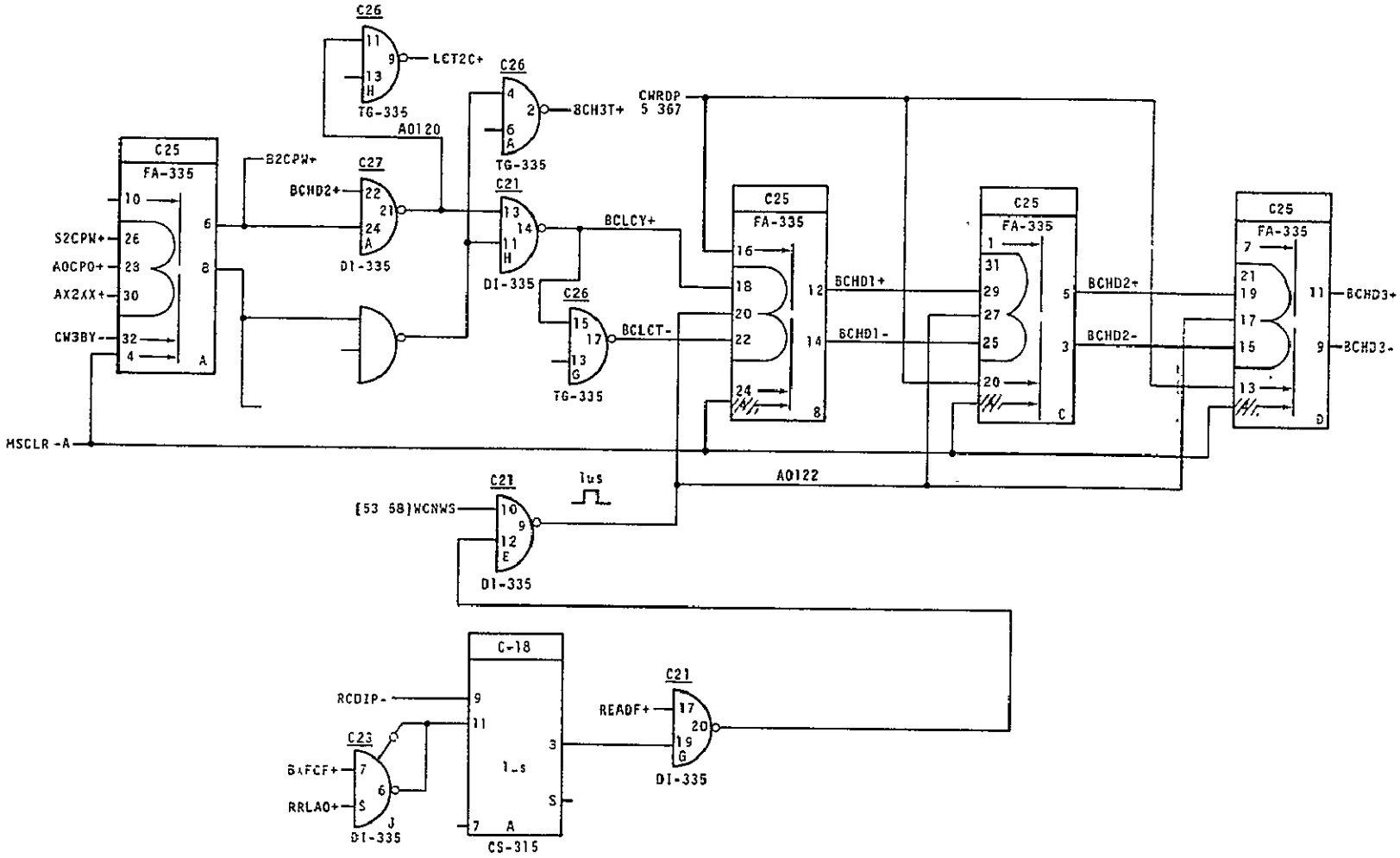


Figure 2-5. — Buffer control.

The logic also determines if the two characters per word mode or the three characters per word mode has been selected. Each segment of the word to be output to the MTT is selected by an appropriate signal; BCHD1+ selects the first group, BCHD2+ selects the second group, and BCHD3+ selects the third or last group if the three characters per word mode has been selected. Each selected group is sent to the lateral parity generator circuit (see figure 2-6) where the 7th parity bit is generated and added to the other 6 bits.

The 6-bit character, BWDB1 through BWBD6, and the lateral parity bit, A0219, are clocked into the read/write register by the write strobe, WCNWS. (See figure 2-7.) The write control file mark strobe, WCFMS, unconditionally sets bits 1, 2, 3, and 4 to 1. This is the octal 17_8 file mark. Gate B18 decodes binary coded decimal (BCD) zero when writing in the two-character per word, BCD, even parity mode and sets bits 2 and 4 to 1. This is then recorded on the tape as an octal 12_8 (1010_2) which is a non-existent BCD code. This is necessary because each character must make at least one flux change on the tape. The circuit in figure 2-8 is used to detect an octal 12_8 on the data read from the tape and convert it to a BCD zero.

Lateral parity error is checked during write by reading after writing. The circuit in figure 2-9 is used to check parity during read-after-write and during reading. If a parity error is detected then the parity error flip-flop (figure 2-10) is set by RSPEF.

Longitudinal parity error is checked by the circuit in figure 2-11. This register is complemented each time a 1 (flux change) is read from the tape. All the flip-flop outputs are "or'ed" together, and if at the end of the record one of the flip-flops is set, the parity error flip-flop will be set. The output of the "or'ed" flip-flops is "and'ed" with the end-of-record pulse

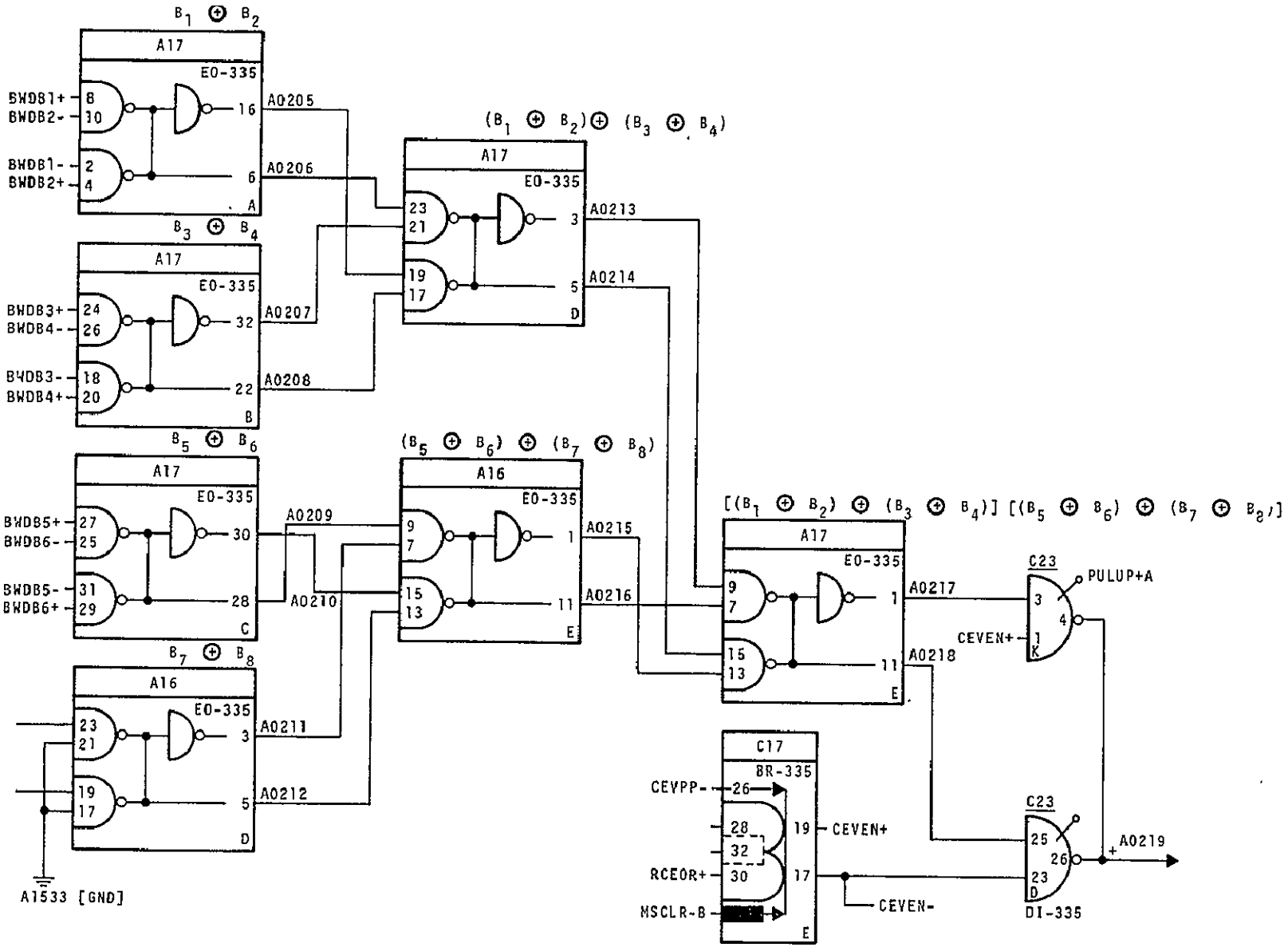


Figure 2-6. — Lateral parity generator.

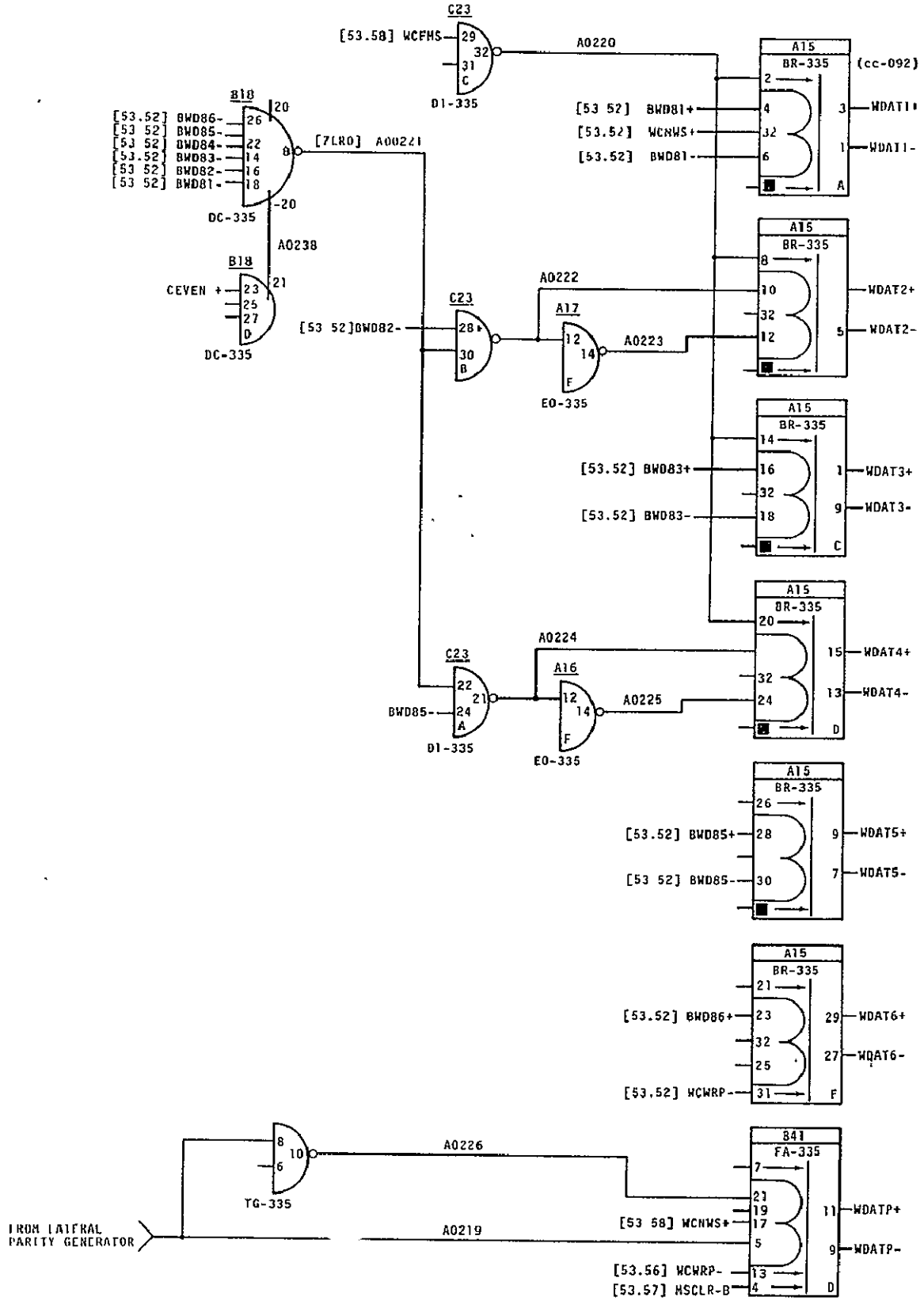


Figure 2-7. — Read/write register.

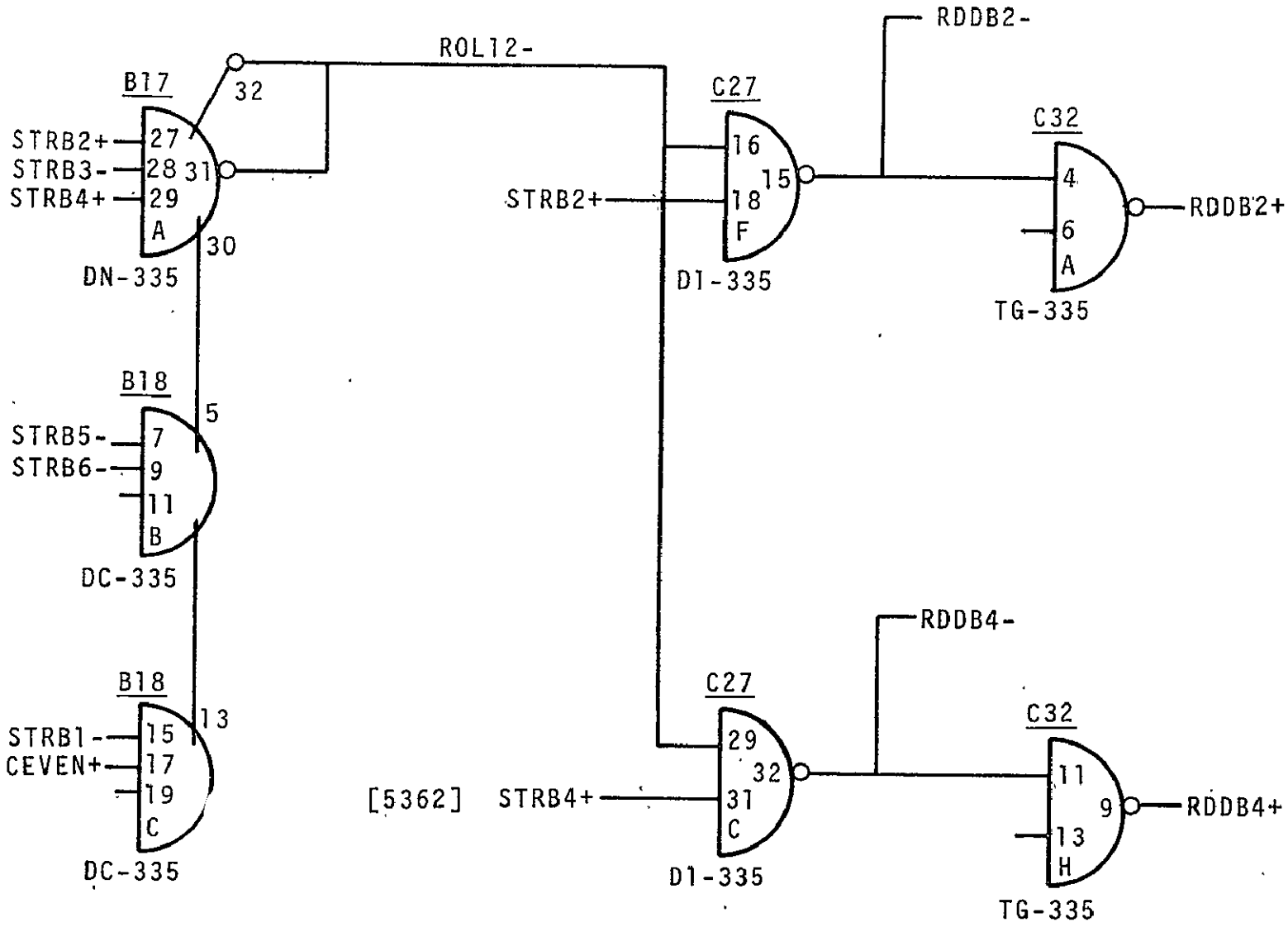


Figure 2-8. — Tape 12_8 to bcd zero detection circuit.

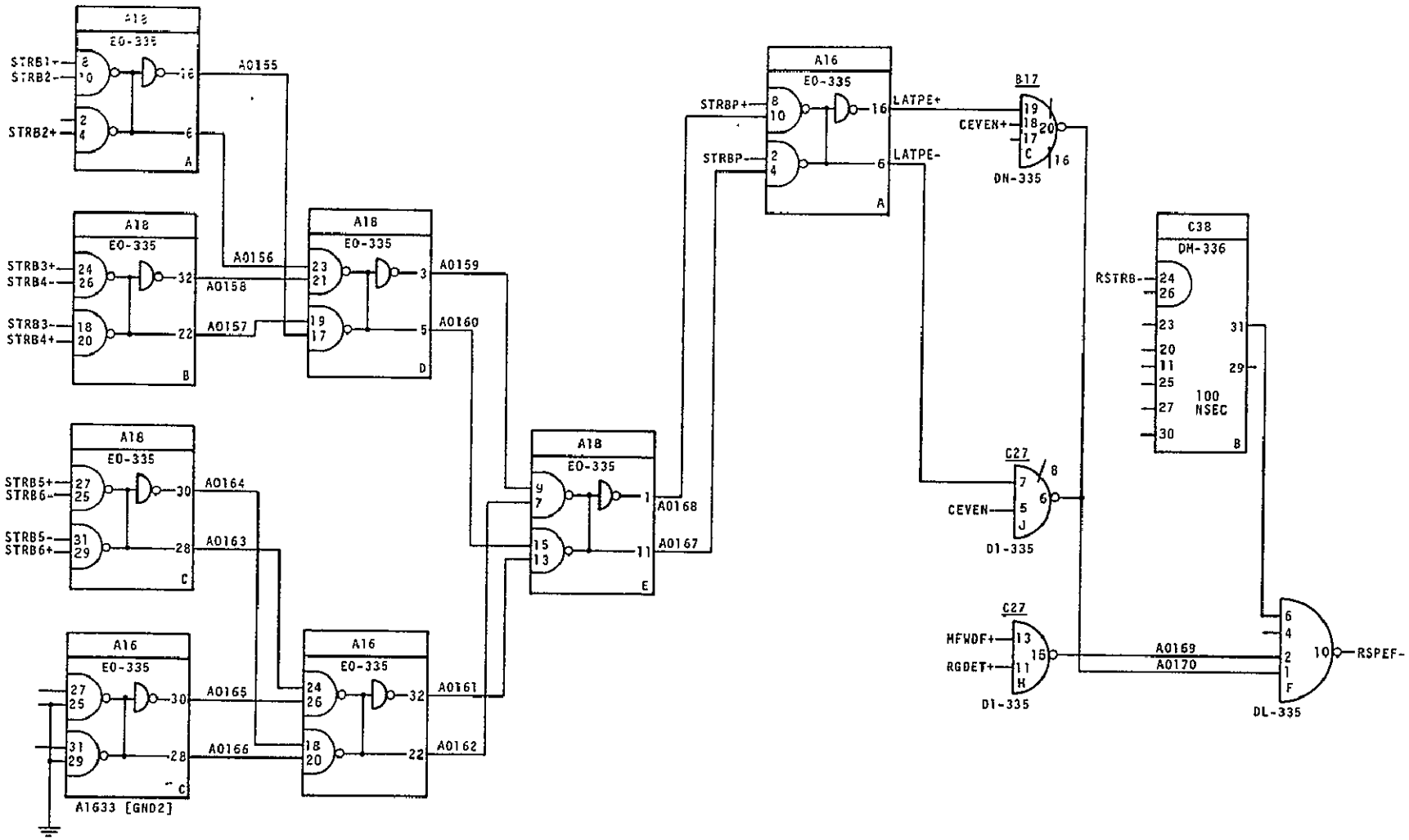


Figure 2-9. — Lateral parity check circuit.

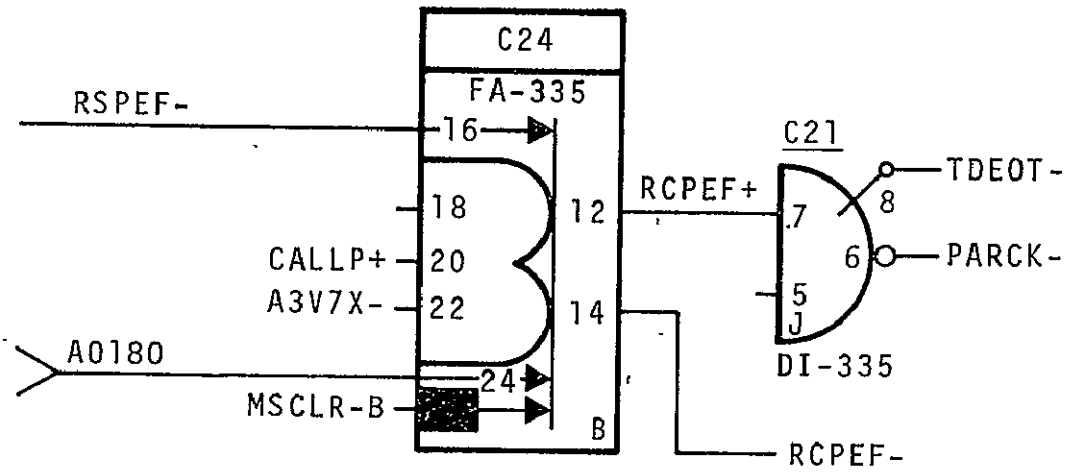


Figure 2-10. Parity error flip/flop.

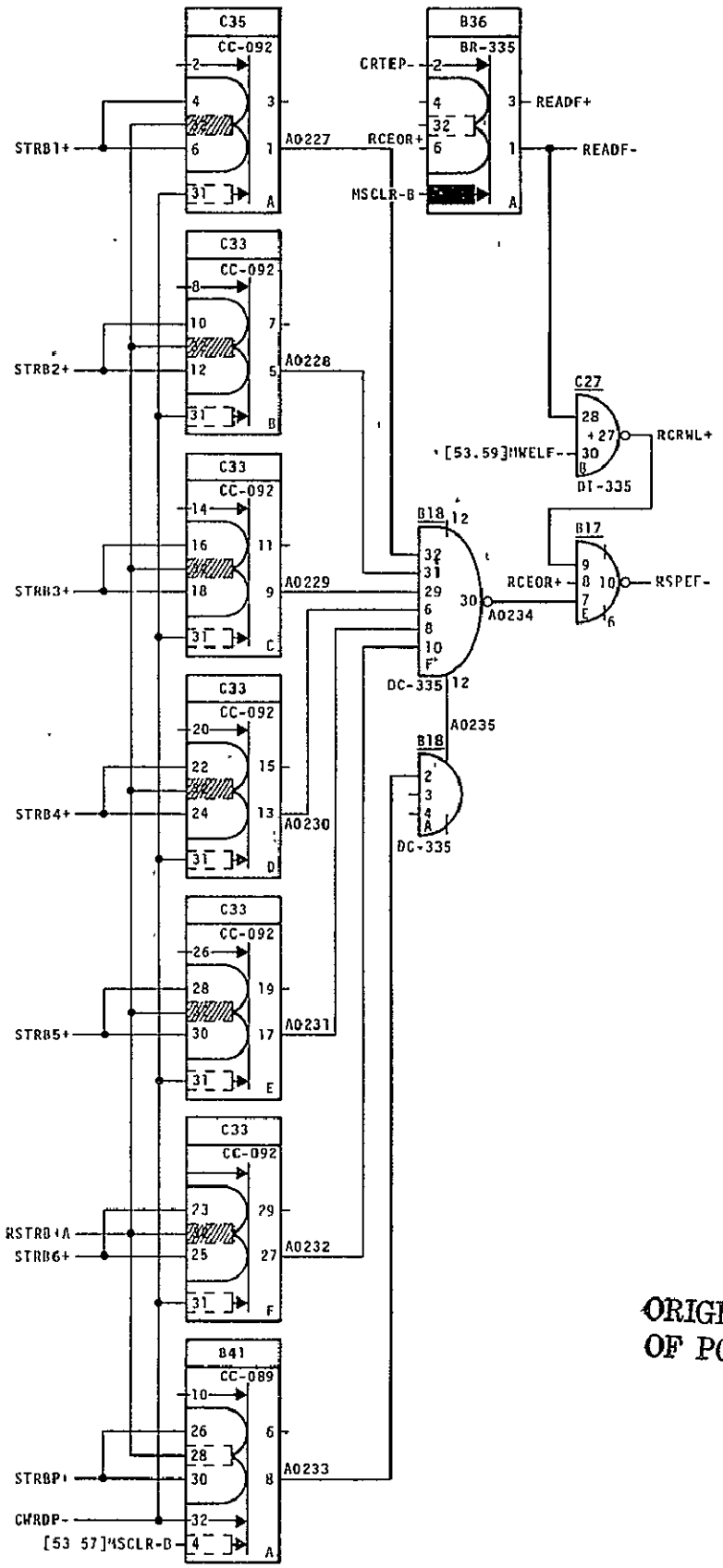


Figure 2-11. — Longitudinal parity error checker.

(RCEOR+) and with the read control read or write level signal (RCRWL+). This signal is present if a read or write operation is being conducted.

The overrun circuit shown in figure 2-12 is used to set the parity error flip-flop in the event the CPU does not honor a data transfer request from the TCU. Normally at the end of each data transfer, RRLAX- signal from the CPU resets the buffer ready flip-flop which is set by CWDAP- or by BXFER-. If RRLAX- does not occur, the buffer ready flip-flop will remain set. This is "and'ed" with the buffer transfer pulse (BXFER+) and the read flip-flop output (READF+). This signal is wired "or" with all other RSPEF- lines to set the parity error flip-flop.

2.3.2 ADDRESS AND CONTROL LOGIC

The MTT address decode logic is shown in figure 2-13. It decodes the last two bits of the address word (bit 15 and 16) to generate one of four output signals. Thus each TCU can operate up to four tape units.

Whenever any write command is issued by the CPU, the first word-forming buffer is reset by a pulse (BCRES-) which is generated by the circuit shown in figure 2-14. The RRLIN- pulse from the CPU is used to generate BTTOE- (Buffer Transfer Output Bus Enabled) which strobes the data from the output bus into the first buffer (figure 2-15). For the first CPU-TCU word transfer, BXFCF, which is set by any write command (figure 2-16) allows RRLAO+ to trigger one shot C18. This pulse is "and'ed" with BXFCF+ to form the input to "or" gate B32. The output of gate B32 is the buffer transfer pulse (BXFER+) which strobes the data from buffer 1 to buffer 2. Subsequent BXFER+ strobe pulse originate from the write strobes (WCNWS-) by way of C21 and "and'ed" with BCLCT+ (Buffer Control Last Character Time). The output equation for BXFER+ is: $(WCNWS + RCDIP)'(BCLCT) + (BXFCF)(RRLAO) + (RGAPD)(READF)(\overline{RGDET})(LCT2C) = BXFER$.

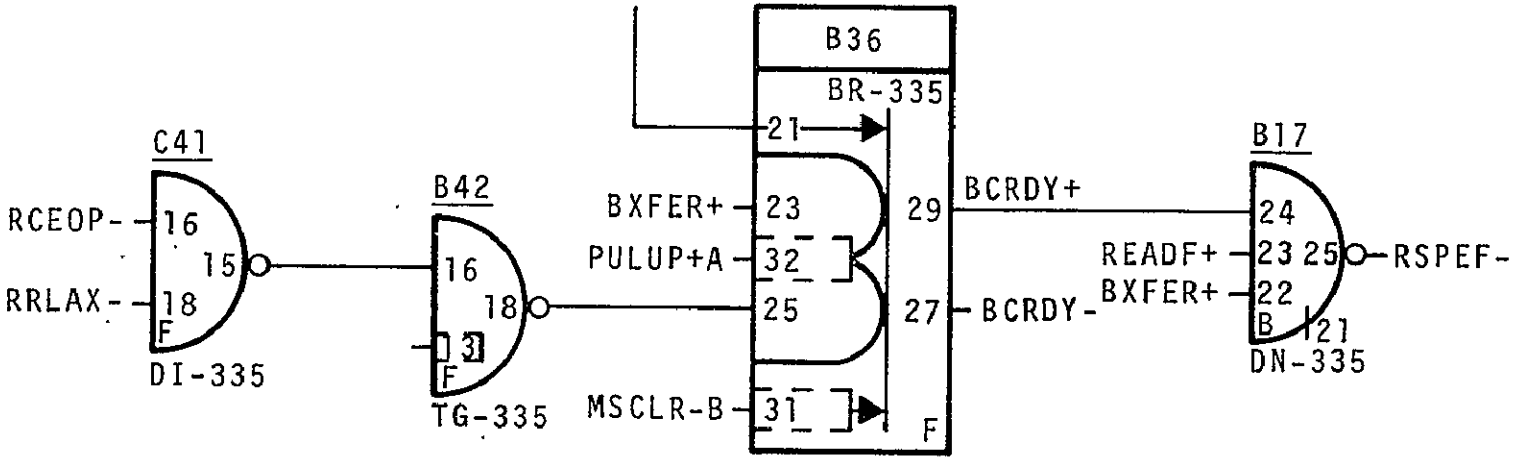


Figure 2-12. — Overrun logic.

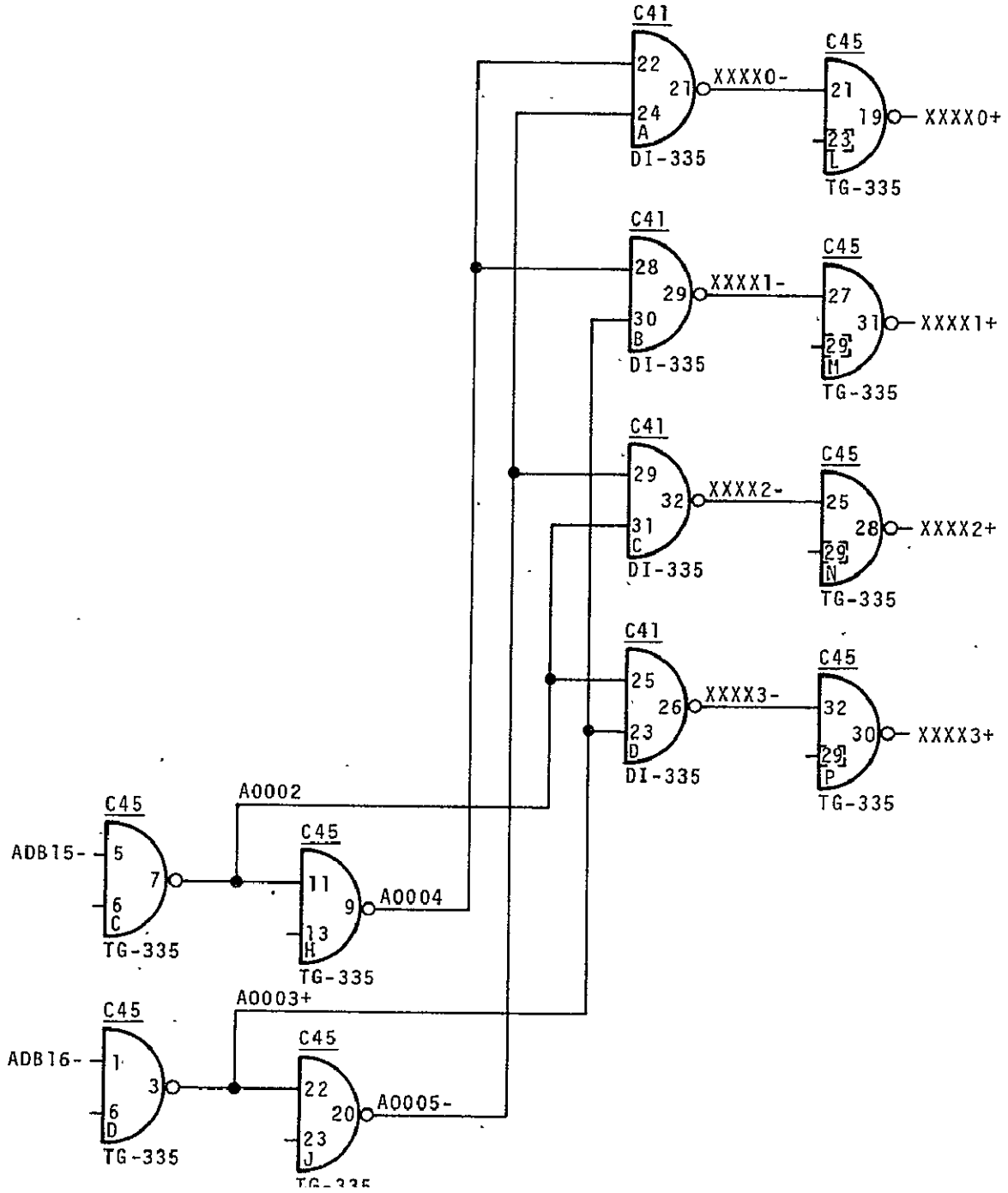


Figure 2-13. — MTT unit number decode logic.

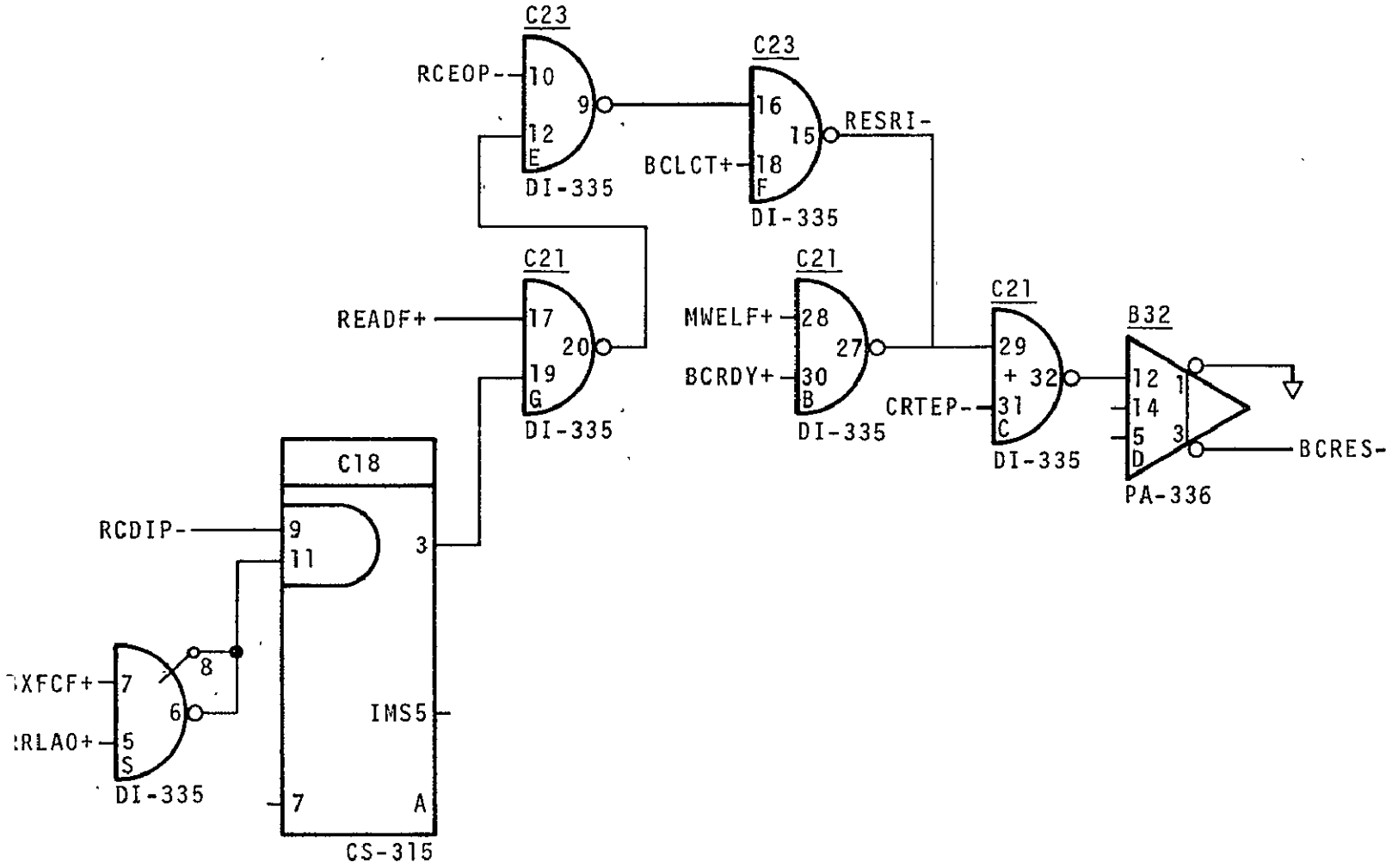


Figure 2-14. — Buffer reset (BCRES-).

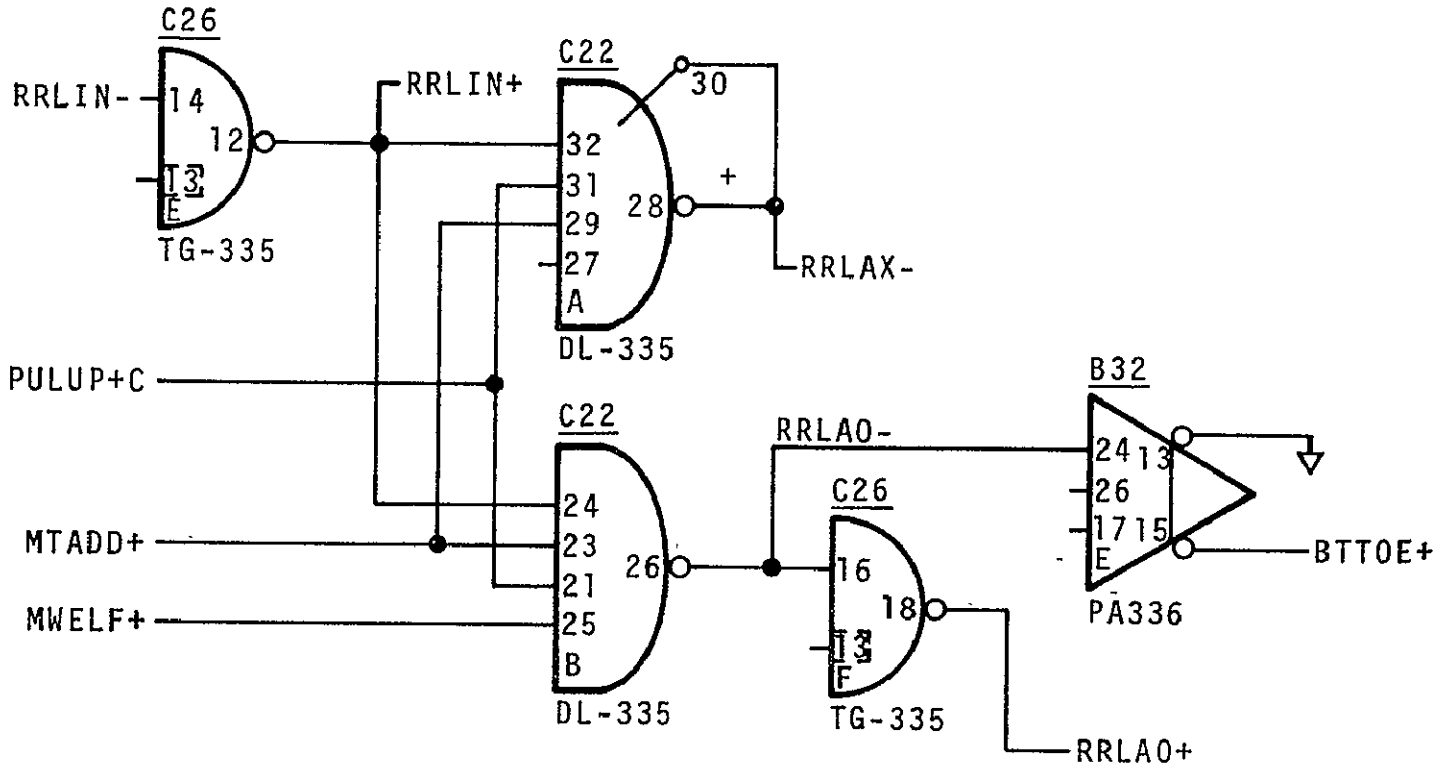


Figure 2-15. — Buffer transfer output bus enable.

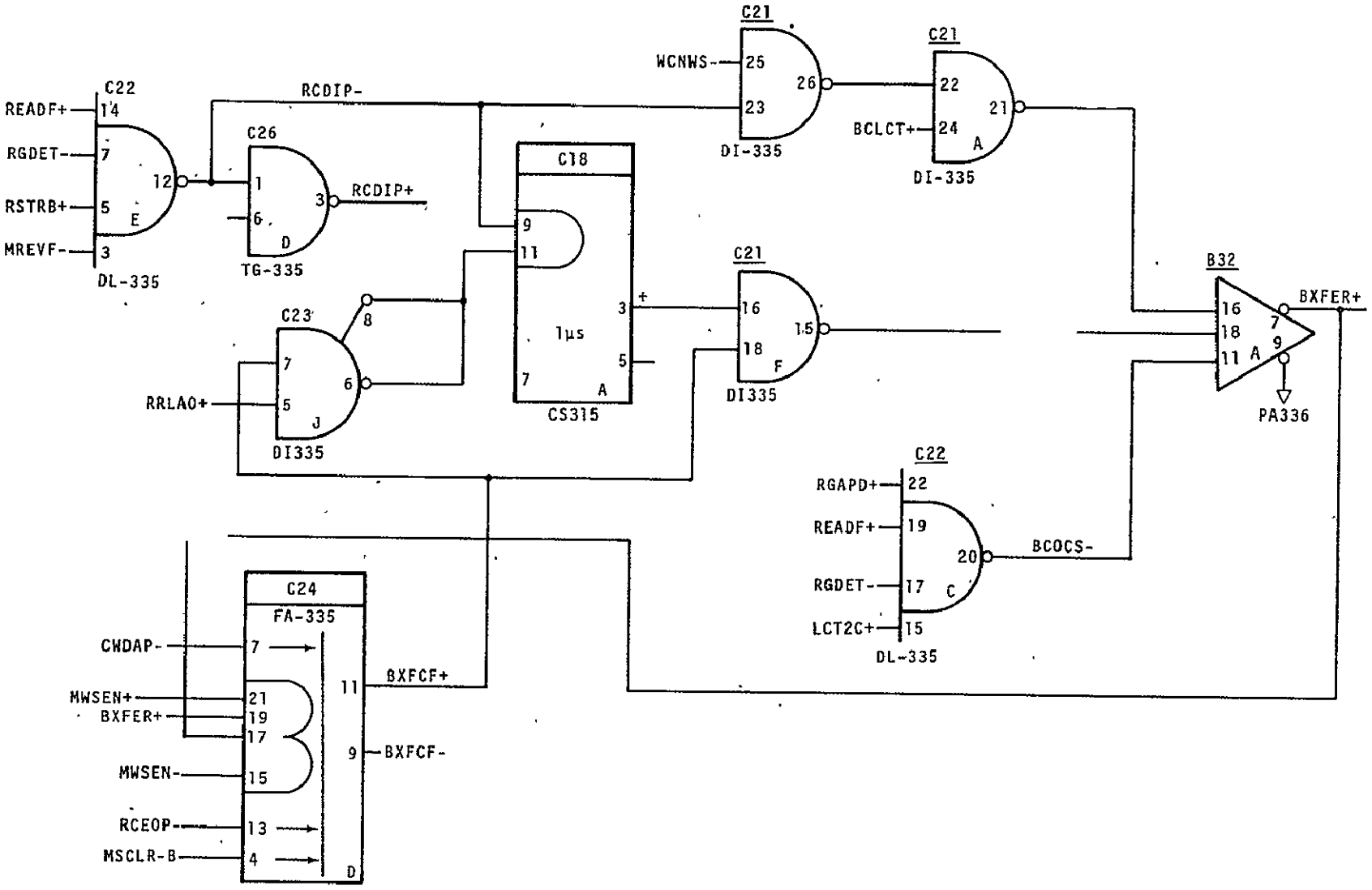


Figure 2-16. — Buffer transfer pulse logic.

Figure 2-17 contains the logic which gates the data from the TCU to the computer input bus. Signal CHSLI+ is generated in the DMC logic and will be discussed later. MTADD+ is formed whenever the TCU is addressed by the CPU and READF+ is formed whenever a read function has been commanded.

The address word transmitted from the CPU is as shown in figure 2-18. Bits 1 through 6 are not used and bits 7, 8, 9, and 10 are used as the function code to tell the TCU what action is required. Bits 11, 12, 13, 14 are used as the TCU address. TCU 1 has address octal 2_8 and TCU 2 has address octal 3_8 or as shown in figure 2-19 ADB13+A and ADB14+A are 1 and ADB11- and ADB12- are zero for TCU 2. The signal MTADD+ is used to indicate that this TCU has been selected. This signal can be generated by gate C44 (figure 2-19) decoding the TCU address from the address bus or by the DMC logic.

Bits 7, 8, 9, and 10 of the address bus are decoded by the function code decode logic shown in figure 2-20. Bits 8, 9, and 10 are decoded by 1 of 8 octal decoder (C44) and those outputs plus their complement are used along with A1XXX and A3V7X to generate the required function signals in the TCU. Signal A3V7X is formed by address bits 9 and 10 and is true whenever a function code contains an octal 3_8 or 7_8.

Command strobe pulses are generated by the circuitry shown in figure 2-21. Signals AOCP1+ and AOCP0+ are used to generate the command signals shown in figure 2-22. The two signals are generated whenever the TCU is addressed and it is not busy. Gate B43 will inhibit AOCP1+ and AOCP0+ whenever the motion-busy status signal (MBSXS+) is true and a function code with a 3_8 or 7_8 in it has not been transmitted by the TCU (see table I for TCU commands). AOCP1+ or AOCP0+ can be generated but not both simultaneously. The status of address bit 7 (ADB07-) is used to generate A1XXX+ and its complement. (See figure 2-20.) These

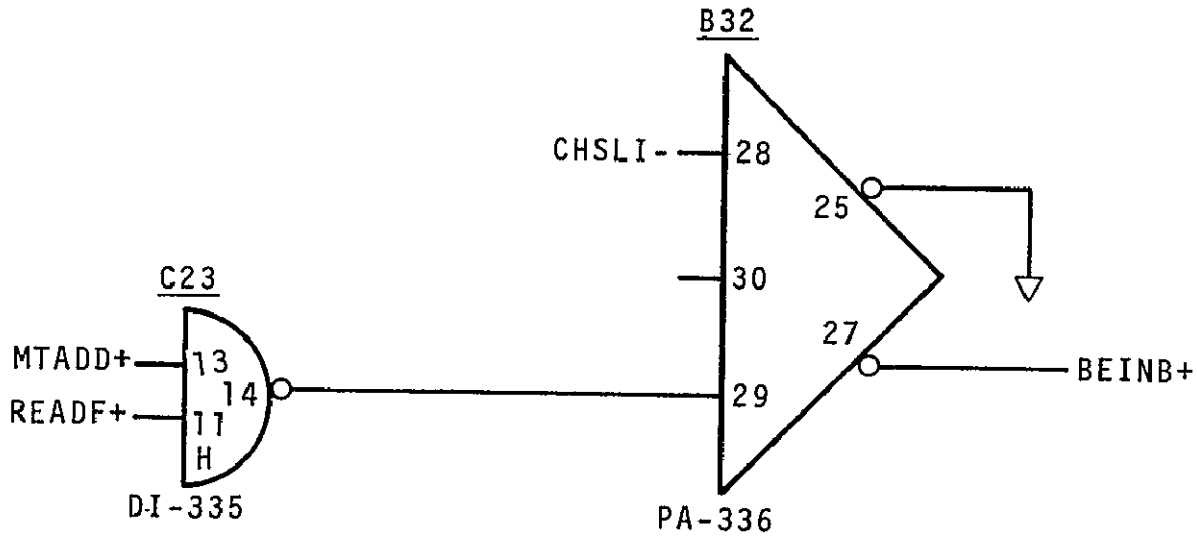


Figure 2-17. – Input bus buffer transfer pulse circuit.

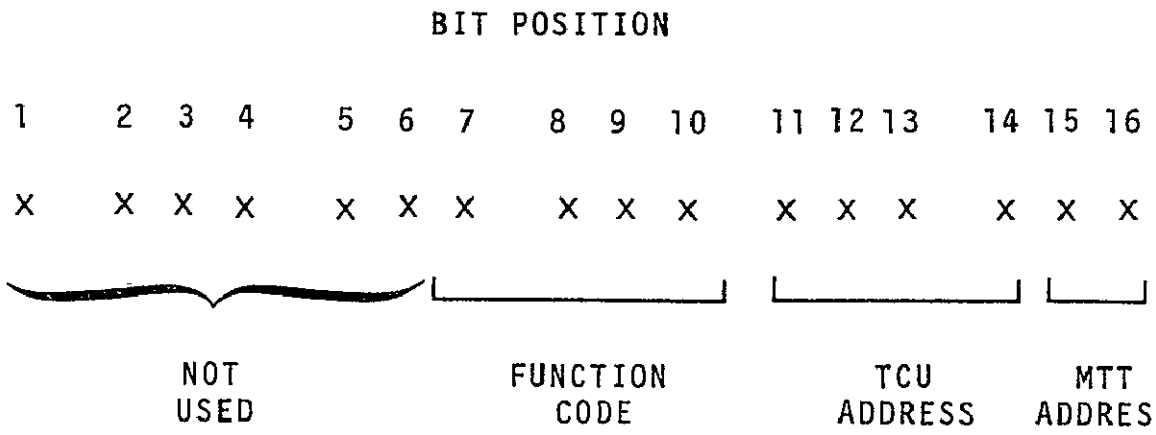


Figure 2-18. — Address word.

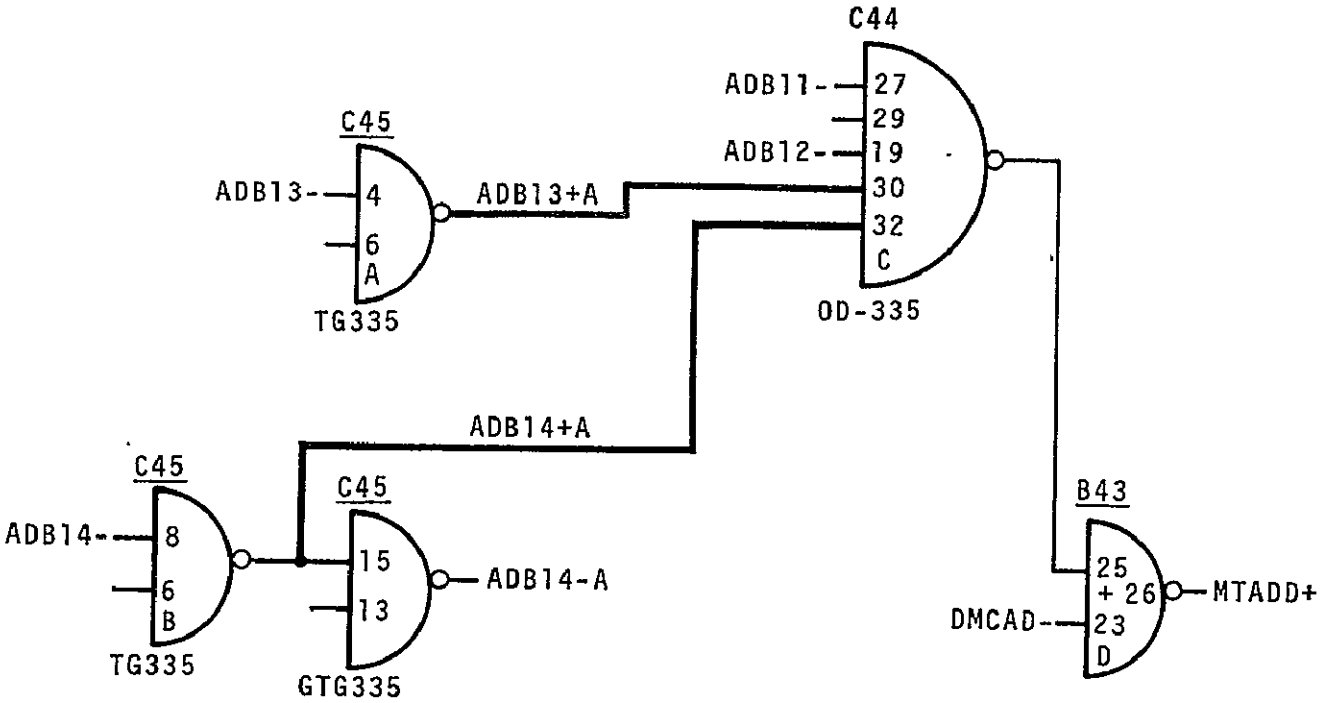


Figure 2-19. — TCU address decode.

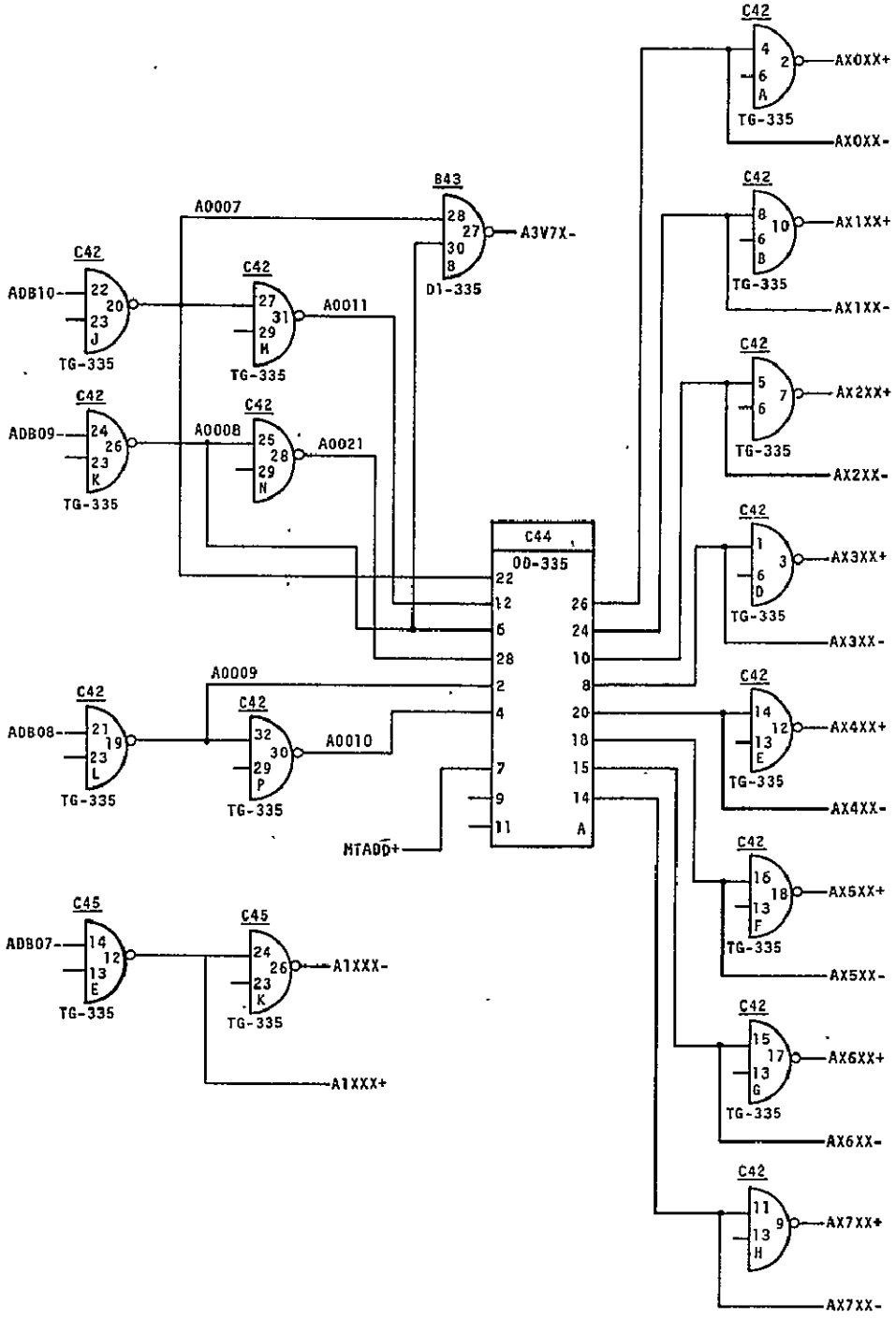


Figure 2-20. — Function code decode logic.

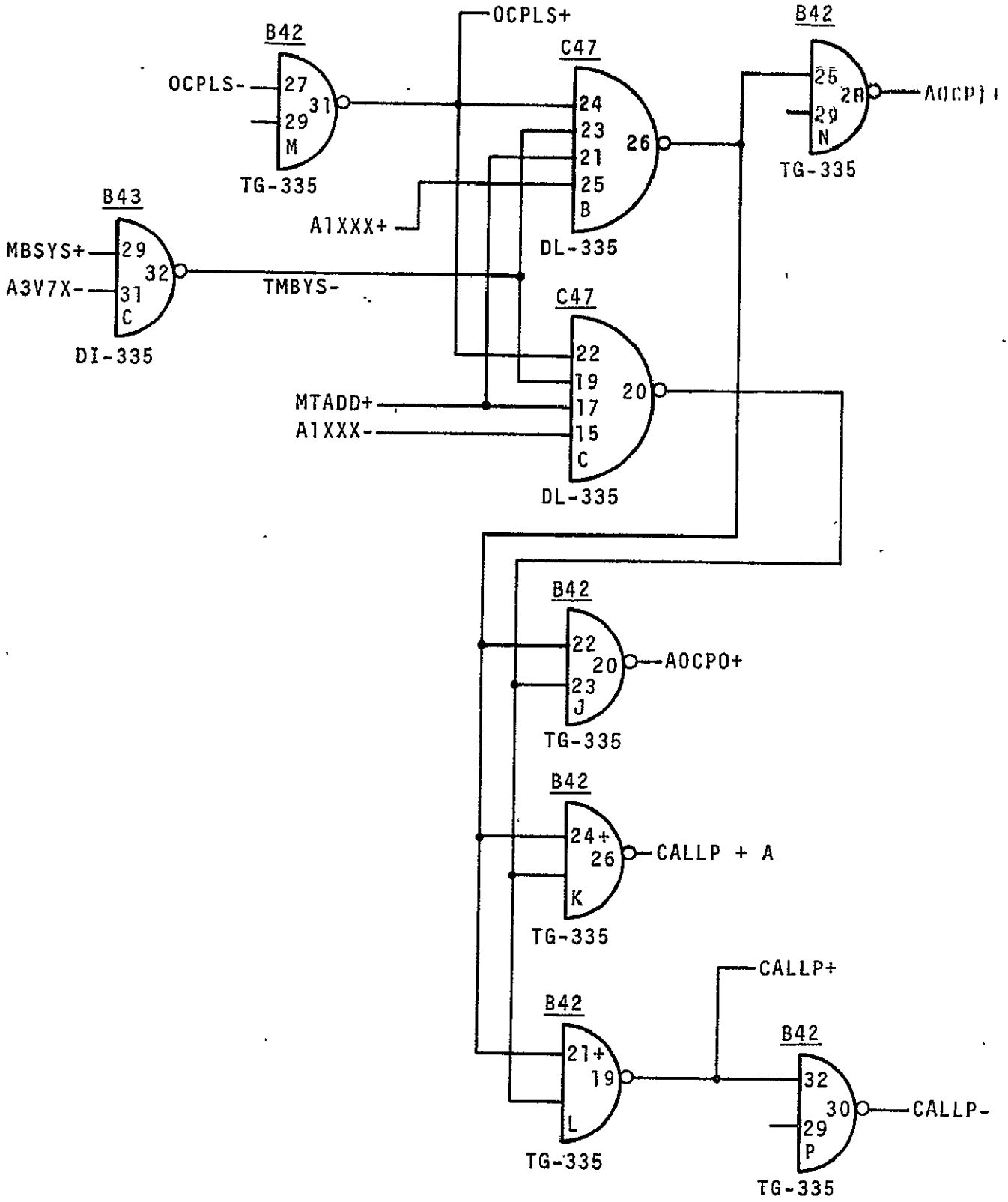


Figure 2-21. — Command strobe pulse circuit.

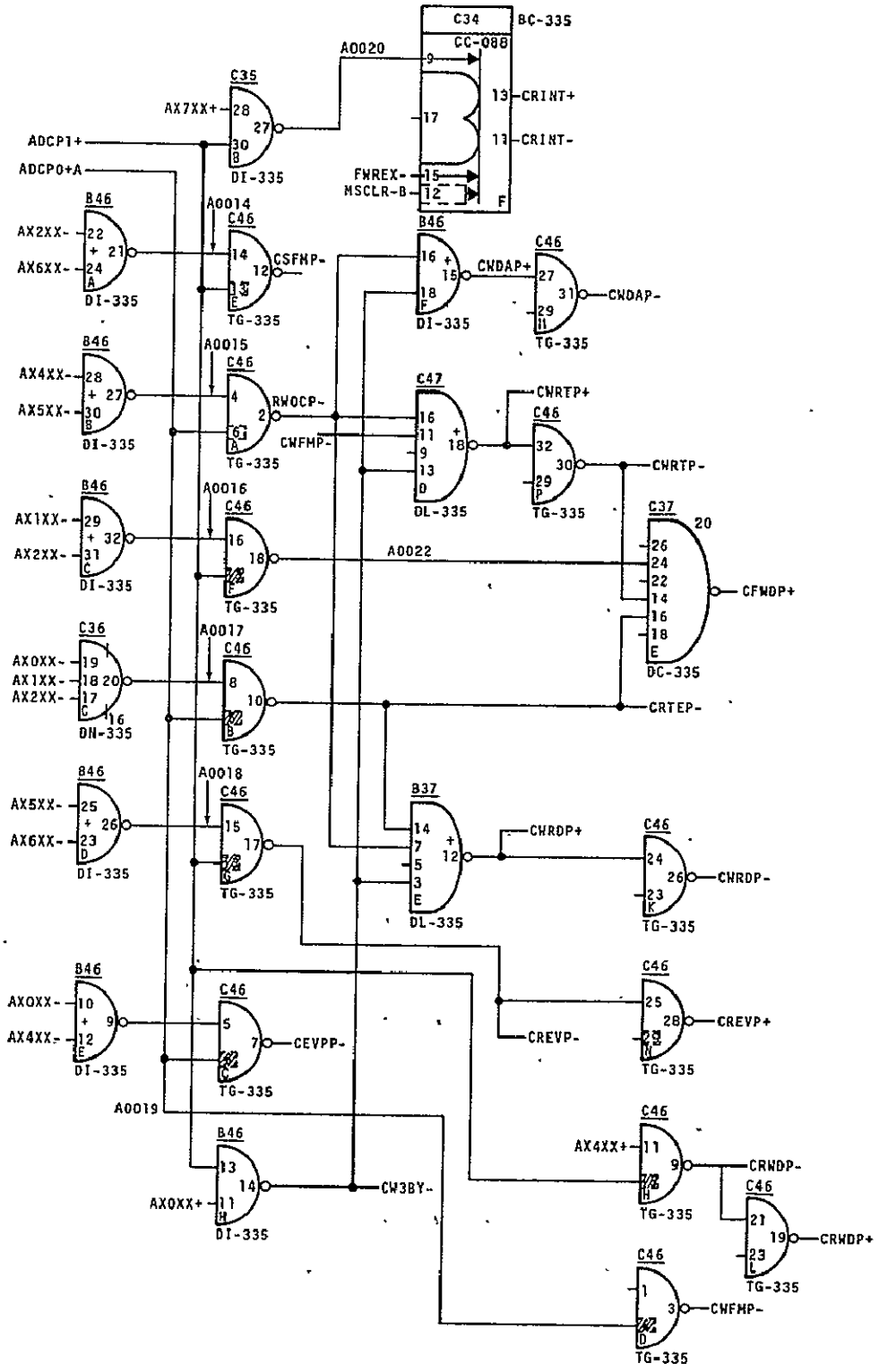


Figure 2-22. — Command signal generation.

TABLE 1.— MAGNETIC TAPE SYSTEMS - MODEL 316/516

Table I contains the function codes for the 7-track TCU.

OCP	1001X	Read BCD, 2 char/word
OCP	′011X	Read binary, 2 char/word
OCP	′021X	Read binary, 3 char/word
OCP	′031X	Set up Normal DMC/DMA mode
OCP	′041X	Write BCD, 2 char/word
OCP	′051X	Write binary, 2 char/word
OCP	′061X	Write end of file
OCP	′071X	Reset DMC/DMA mode
OCP	′101X	Write binary, 3 char/word
OCP	′111X	Space forward one record
OCP	′121X	Space forward one file
OCP	′131X	Set up DMC/DMA in Auto Switch mode
OCP	′141X	Rewind
OCP	′151X	Backspace one record
OCP	′161X	Backspace one file
OCP	′171X	Stop write
SKS	′001X	Skip if ready
SKS	′011X	Skip if not busy
SKS	′021X	Skip if an error has not been detected
SKS	′031X	Skip if not at beginning of tape (load point)
SKS	′041X	Skip if not interrupting
SKS	′051X	Skip if end of tape has not been detected
SKS	′061X	Skip if end of file has not been detected
SKS	′071X	Skip if writing is permitted
SKS	′111X	Skip if MTT operational
SKS	′121X	Skip if DMA/DMC subchannel is not currently processing channel 2
SKS	′131X	Skip if DMC/DMA subchannel is not in Auto Switch mode
SKS	′141X	Skip if not rewinding
INA	′001X	Input from TCU if ready
INA	′101X	Clear "A" register and input from TCU if ready
OTA	′001X	Output data to the TCU
SMK	′0020	Set TCU Interrupt Mode, (A_1) for TCU 1, (A_2) for TCU 2

two signals will only allow one or the other AOCPXX pulses to be generated. If either AOCPXX pulse is generated a general housekeeping pulse, CALLP, will be generated.

The decoded function code signals AXOXX through AX7XX along with AOCP1+ and AOCP0+ are used to generate all required command signals used in the TCU. This is shown in figure 2-22. These signals are also used to generate the device ready signal (DRLIN-) which is sent to the CPU in response to any SKS, INA, and OTA instruction if the rsponse or condition is true. This is shown in figure 2-23.

During DMC mode operations the CPU will honor interrupt from various devices. When the CPU has found the device which is interrupting, it will prevent other devices from interrupting by masking them off. This is done by outputing a key 16-bit word on the output bus with the set mask (SMK) instruction. In the case of TCU 2, if output bus bit 2 (OTBO2+) is true this will cause the mask flip-flop (B41B, figure 2-24) to be set, thus, preventing any interrupts from TCU 2. If bit 2 had been false the mask flip-flop would have been reset, thus, enabling interrupts.

2.3.3 READ LOGIC

Any read command sets the forward motion and read control flip-flops, resets the LRC register, and resets the word-forming buffer. As the tape moves under the read head, data is transferred to the selection logic. As each frame is read, a dropin pulse (figure 2-25) is sent to the work-forming buffer control shift register (see figure 2-26, shift pulse; and figure 2-27, buffer control shift register). When the right number of shift pulses, as controlled by the mode flip-flop (figure 2-28), has occurred the BCRDY flip-flop is set. This causes transfer of one data word to the CPU via the input bus. The CPU issues RRLIN- which resets the BCRDY flip-flop (see figure 2-29). All data

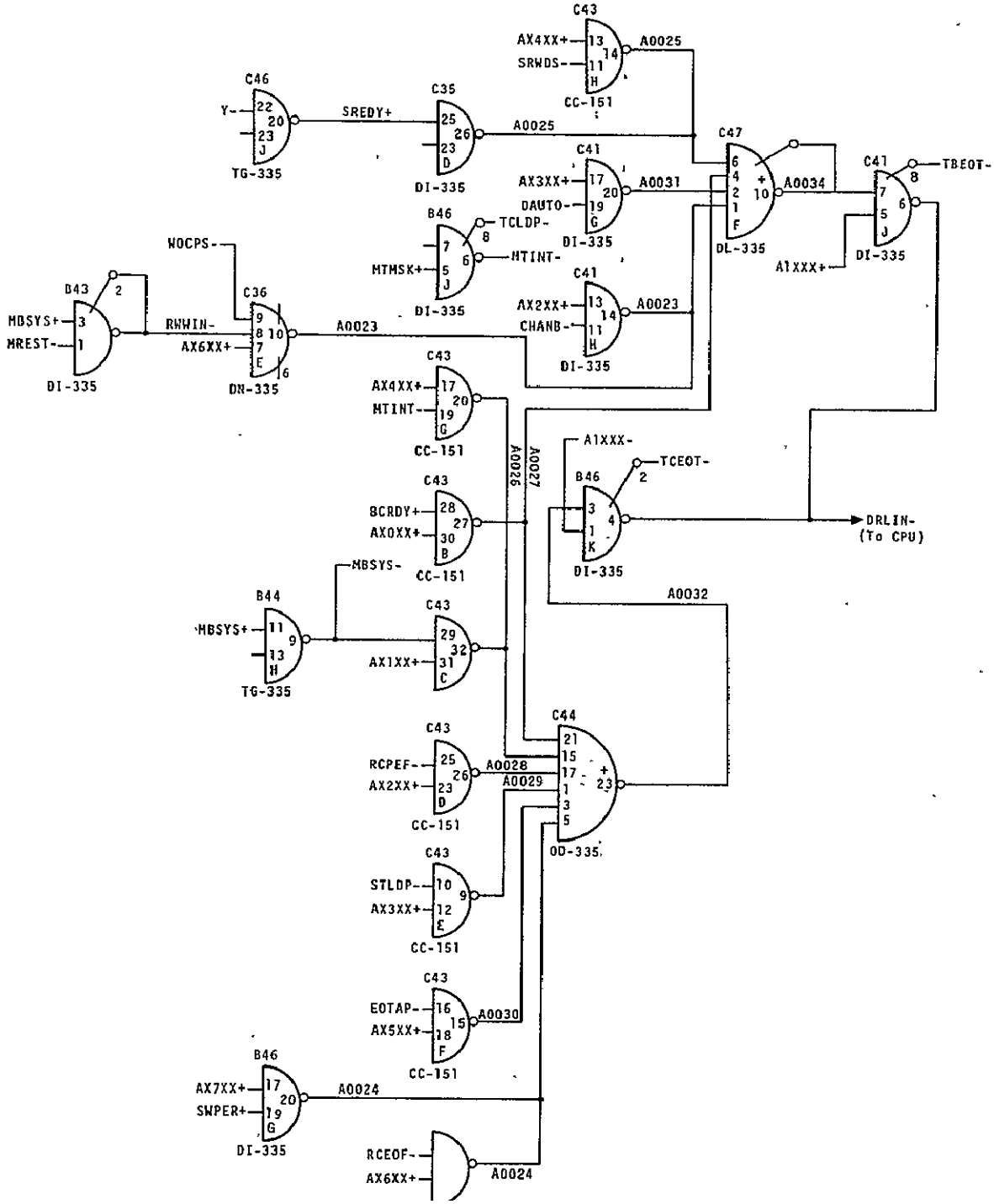


Figure 2-25. — Handshake logic.

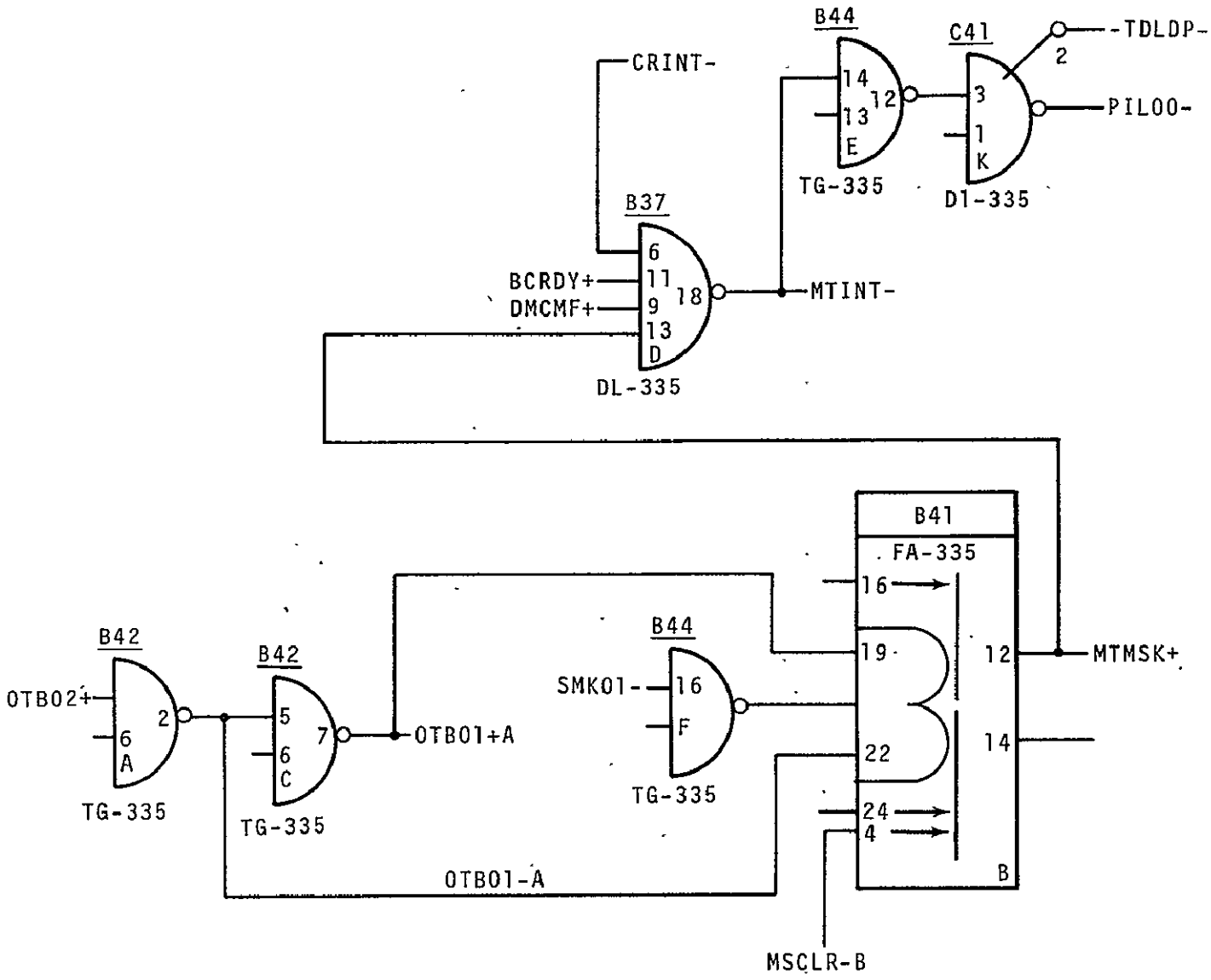


Figure 2-24. — Interrupt logic.

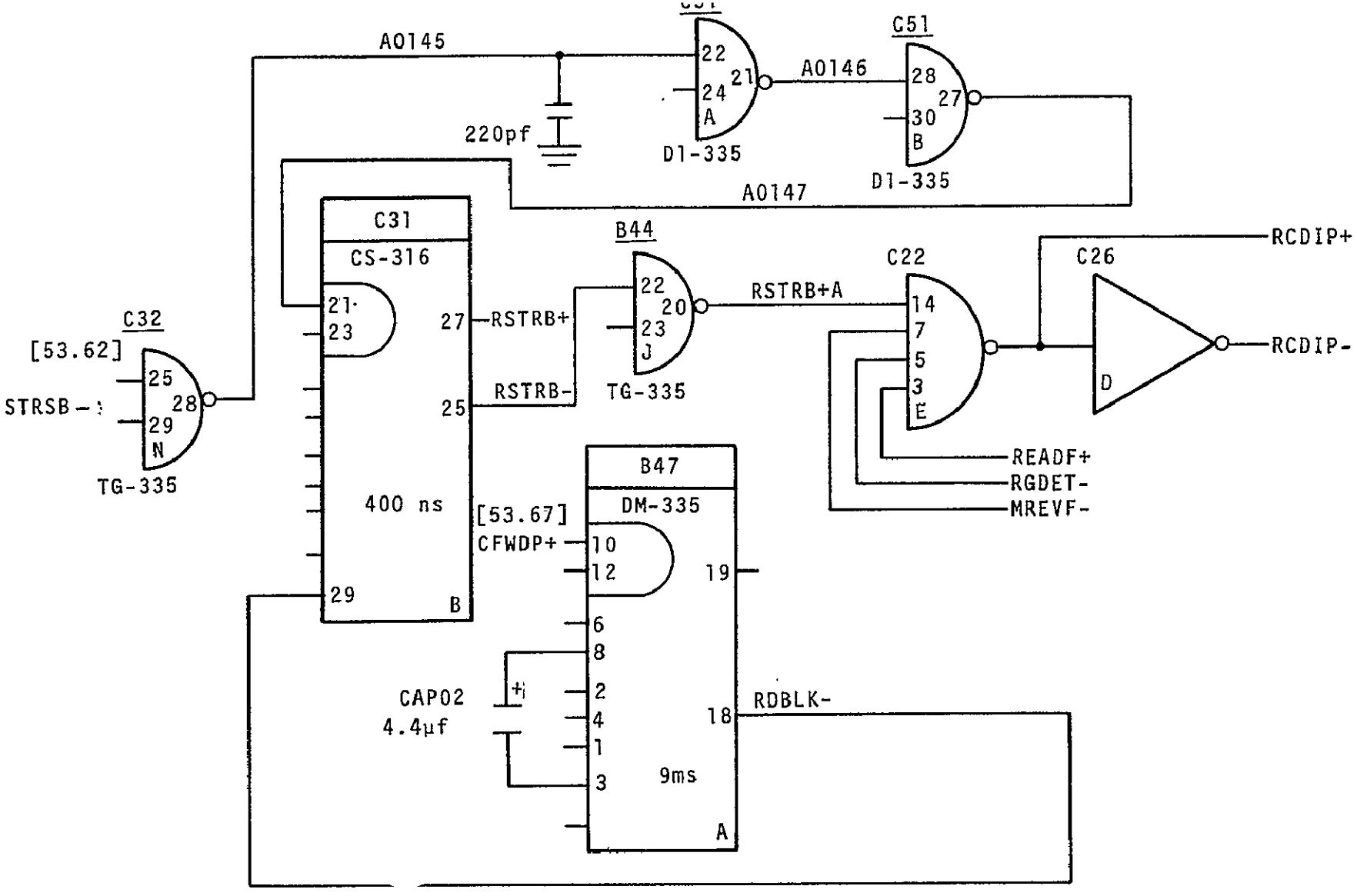


Figure 2-25. — Dropin pulse generation.

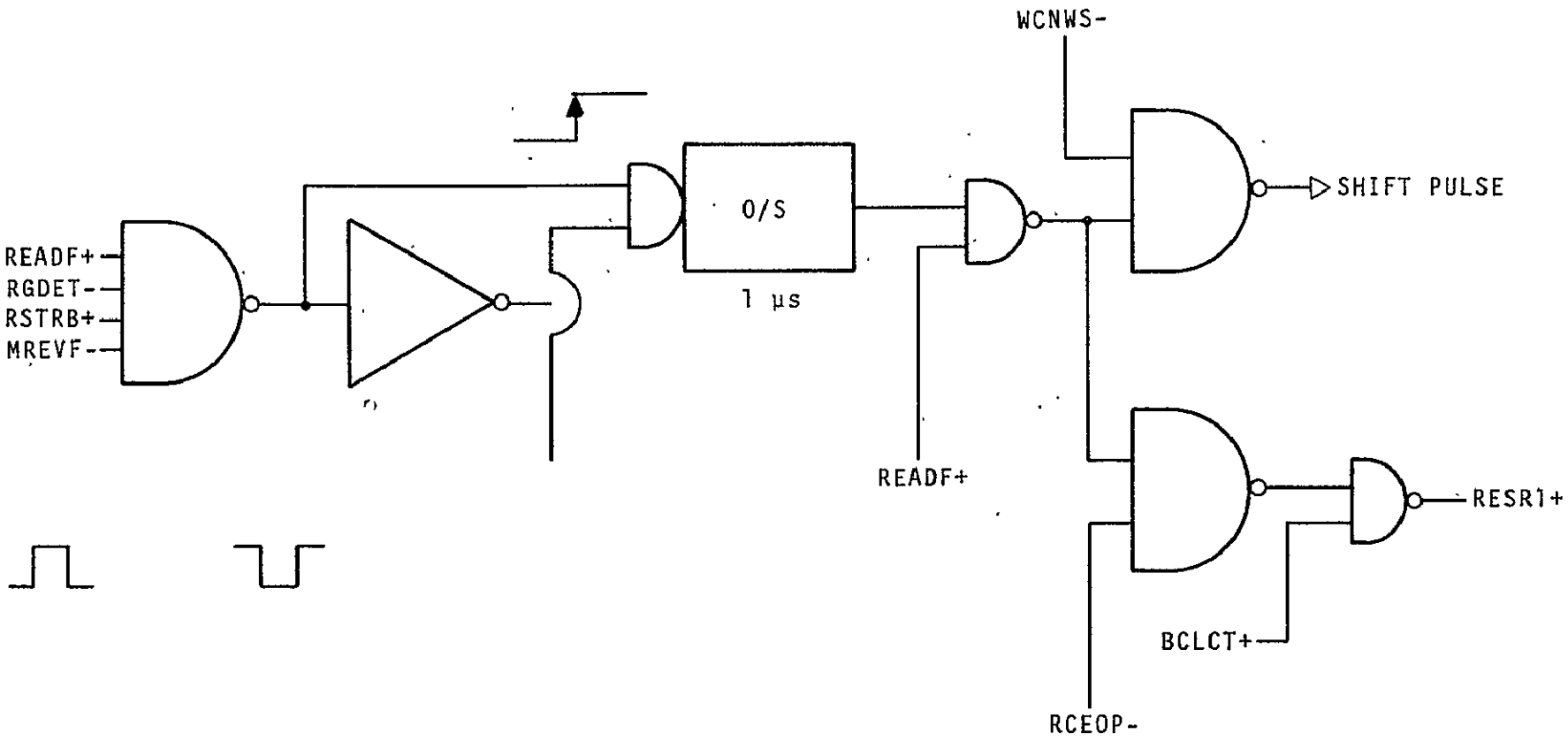


Figure 2-26. — Shift pulse.

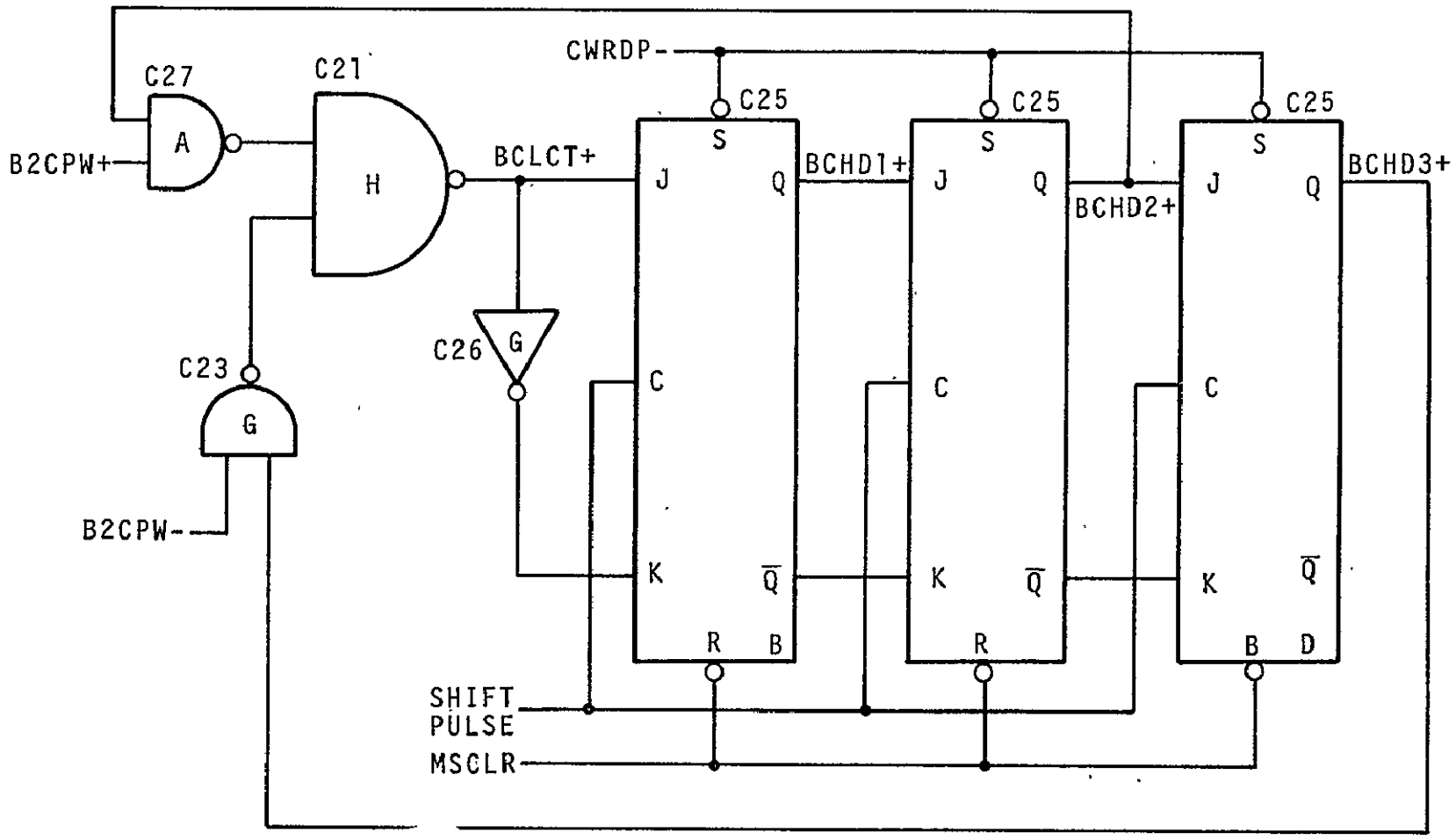


Figure 2-27. — Buffer control shift register.

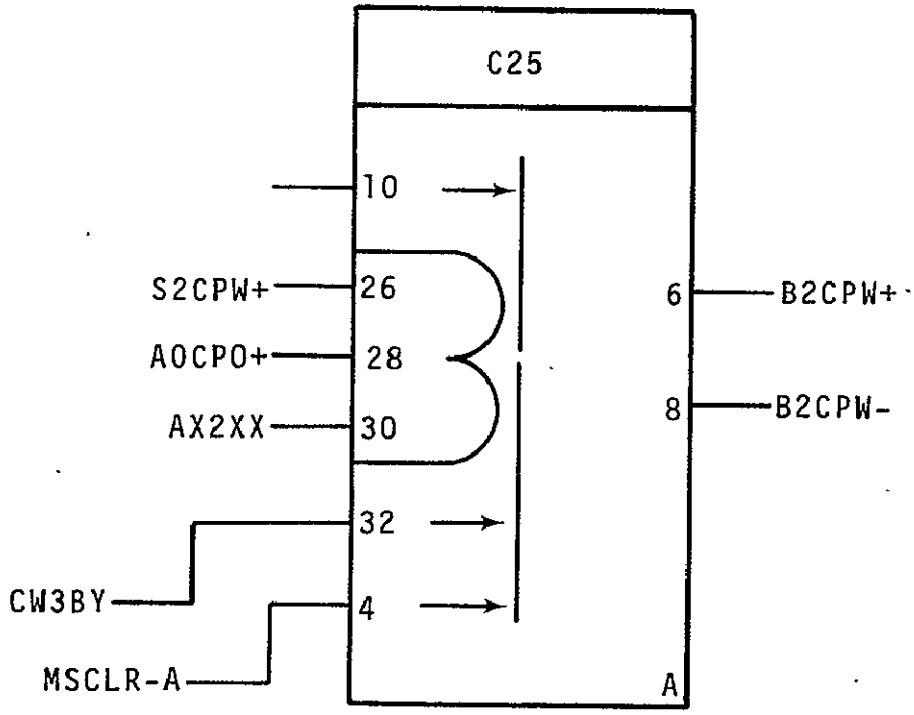


Figure 2-28. — Mode control flip-flop.

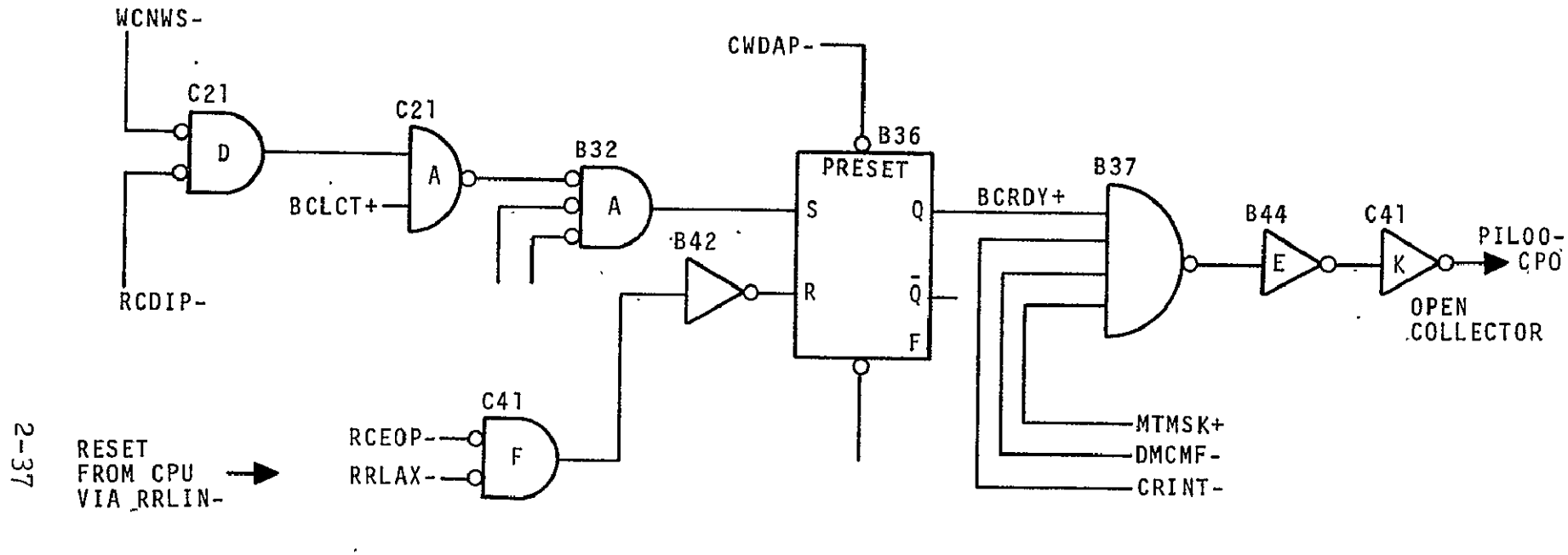


Figure 2-29. — Word transfer enable.

transfer is stopped when the gap between the record proper and the LRC character is detected, this is done by having the RCEOP signal reset the BCRDY flip-flop.

Lateral parity is checked in the parity pyramid consisting of exclusive "or" gates as shown in figure 2-6 and is compared to the state of the parity bit (STRBP). If lateral parity is found to be in error, the read control parity error flip-flop (RCPEF, figure 2-10) is set, enabling that condition to be sensed by the CPU.

The logic shown in figure 2-30 is used to detect an end-of-file mark on the tape and sets a file mark detect flip-flop (RCFMD). If an end-of-record gap is detected while the RCFMD flip-flop is set, an end-of-file flip-flop (RCEOF) is set and the parity error flip-flop is reset.

The read control search file mark flip-flop (RCSFM figure 2-31) is used in generating the end-of-operation signal (RCEOP). If RCSFM is set as a result of a search-for-file mark output control pulse (OCP), signal RCEOP is generated as soon as RCFMD is set and the end-of-record gap has been detected. If a search-for-file mark has not been requested, the RCSFM remains reset and RCEOP is generated as soon as the end-of-record gap (RCEOR) is detected. See figure 2-31, gate C35 where RCSFM- is "and'ed" with RCEOR+ to form RCEOP-.

Read strobe pulses from the selected MTT are shaped by the circuitry shown in figure 2-25. The one shot (C31) is tiggered by the read strobe (STRSB) in both the read and write modes. The signal is used in the write mode for read-after-write operations. The read strobe one shot C31 (RSTRB) is inhibited during any motion for the first 9 to 10 milliseconds of tape travel by one shot (B47). This is to prevent any noise which is under the read head and in the no-record gap from being interpreted as data.

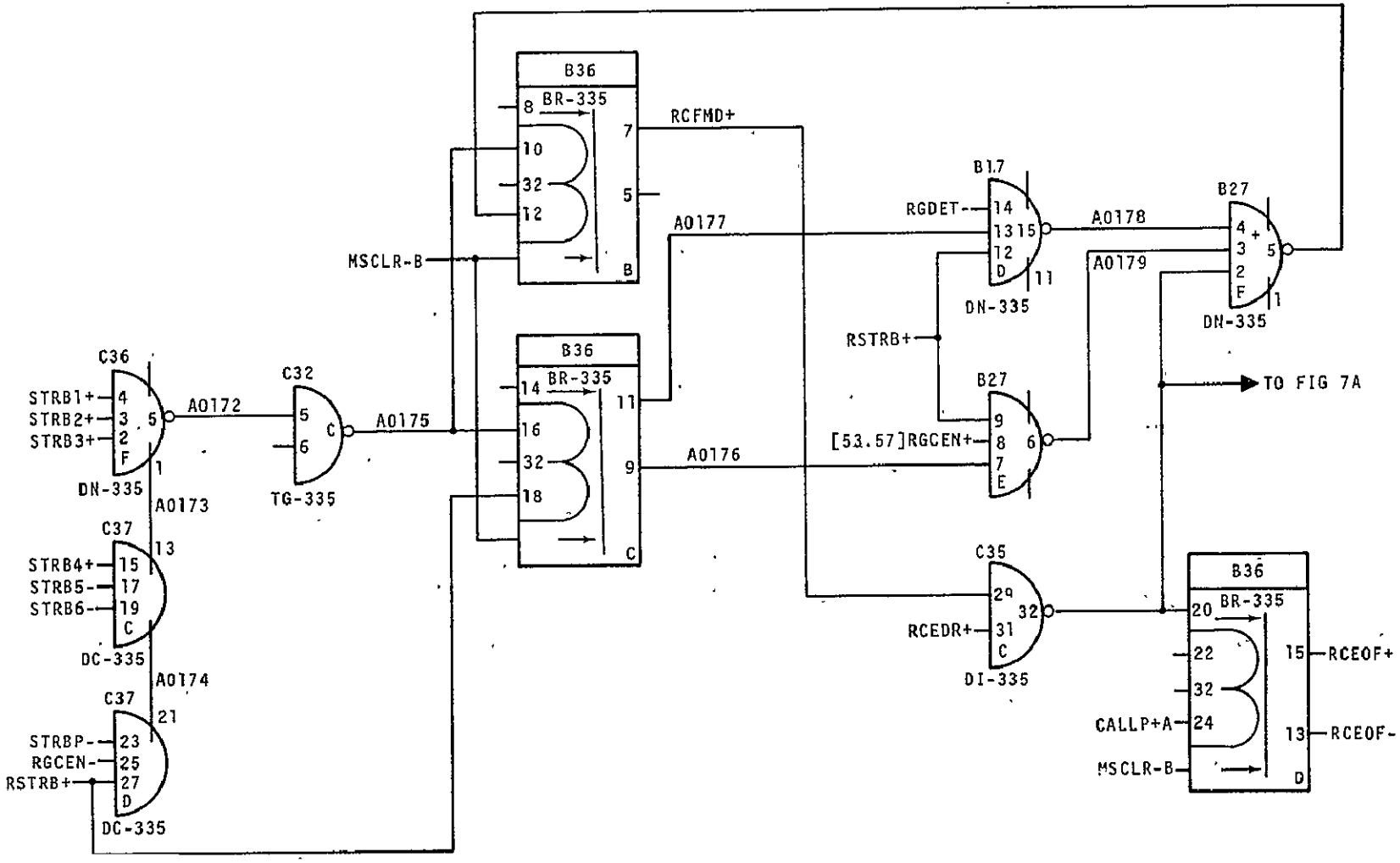


Figure 2-30. — End-of-file detection.

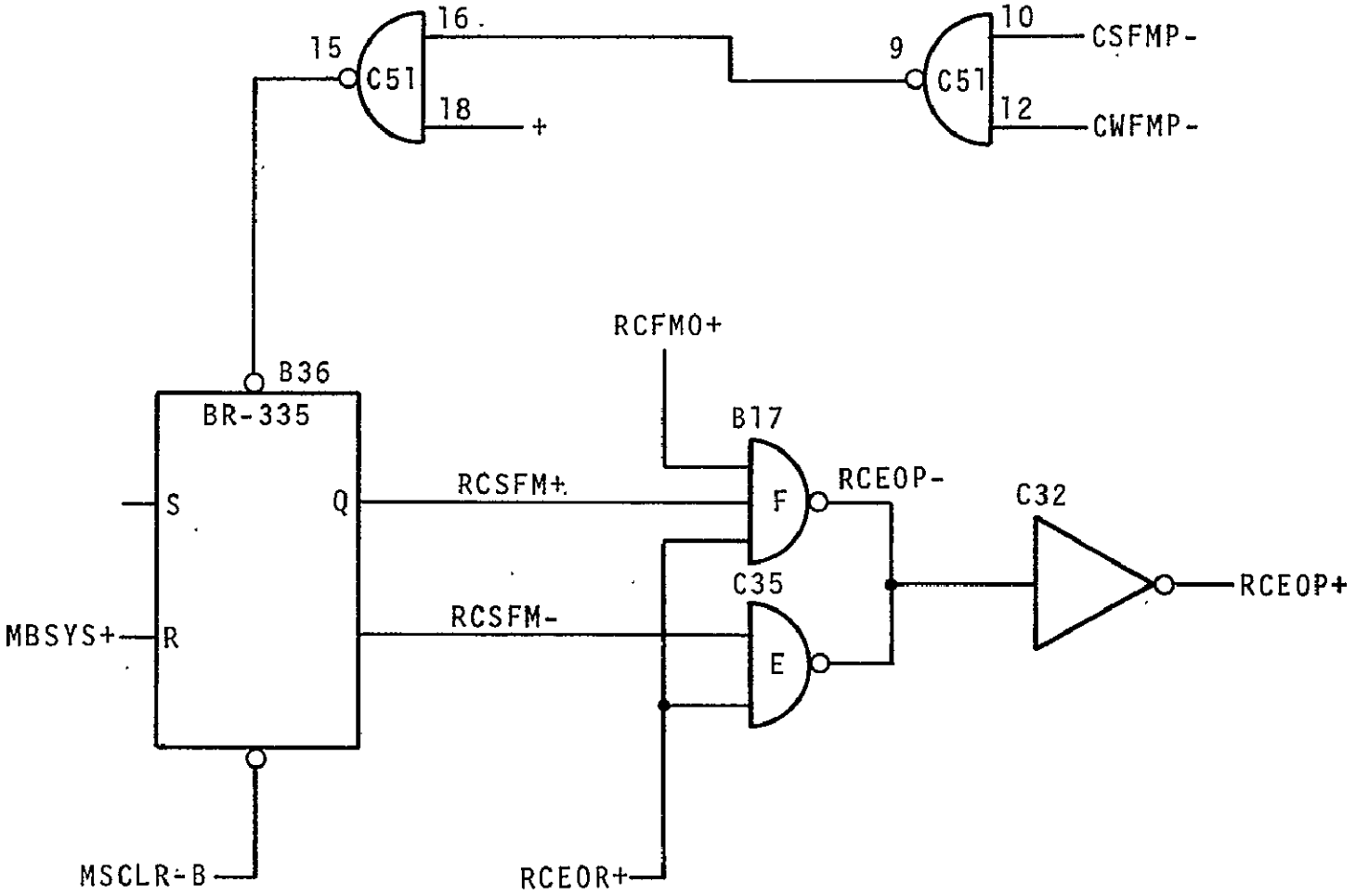


Figure 2-31. — Read control end-of-operation circuit.

The output of the one shot RSTRB is used to set the gap counter (figure 2-32) to all ones by way of signal RGSSY- (figure 2-33). The read strobe pulse (RSTRB) sets flip-flop B35E (figure 2-33). This flip-flop enables the J_1 input of flip-flop B42 (record gap set synchronize flip-flop, RGSSY) which is set on the first positive pulse of the write clock signal (WCCLK+). RGSSY- then sets flip-flop B35(F) which enables the record gap counter by way of signal RGCEN+.

When the record gap counter enable flip-flop (RGCEN) is set this allows the record gap counter to count up at the clock rate (WCCLK-, see gate C35H figure 2-32) which is twice the frame rate. If no more read pulses are received the counter continues to count up until it reaches 00101_2 which indicates that a record gap has been detected and generates signal RGAPD+ (see gate B27A, C37A, and C32M; figure 2-32). This signal sets flip-flop B35A (see figure 2-34) which generats the record gap detected signal (RGDET+). If another read strobe is detected after the RGDET flip-flop has been set, gates C22D and C32K will set flip-flop B35B (see figure 2-34). This will set the parity error flip-flop (see figure 2-10).

A timing diagram of the gap detection circuit is shown in figure 2-35. Whenever a read strobe is late by more than 1-1/2 periods RGAPD is generated. Any read strobes after this point will cause the parity error flip-flop to be set. However, if a RCEOR is generated it will signal a correct end-of-record gap and will reset flip-flop B35B (figure 2-34) thus preventing the parity error flip-flop from being set. Flip-flop B35B provides one read strobe storage to provide for the longitudinal parity error check character. The RCEOR is generated when the gap counter reaches 111101_2 by gates C36D, C37B, and B42E as shown in figure 2-33. This signal (RCEOR) is used to generate the read control end-of-operation signal (RCEOP) as shown in figure 2-31.

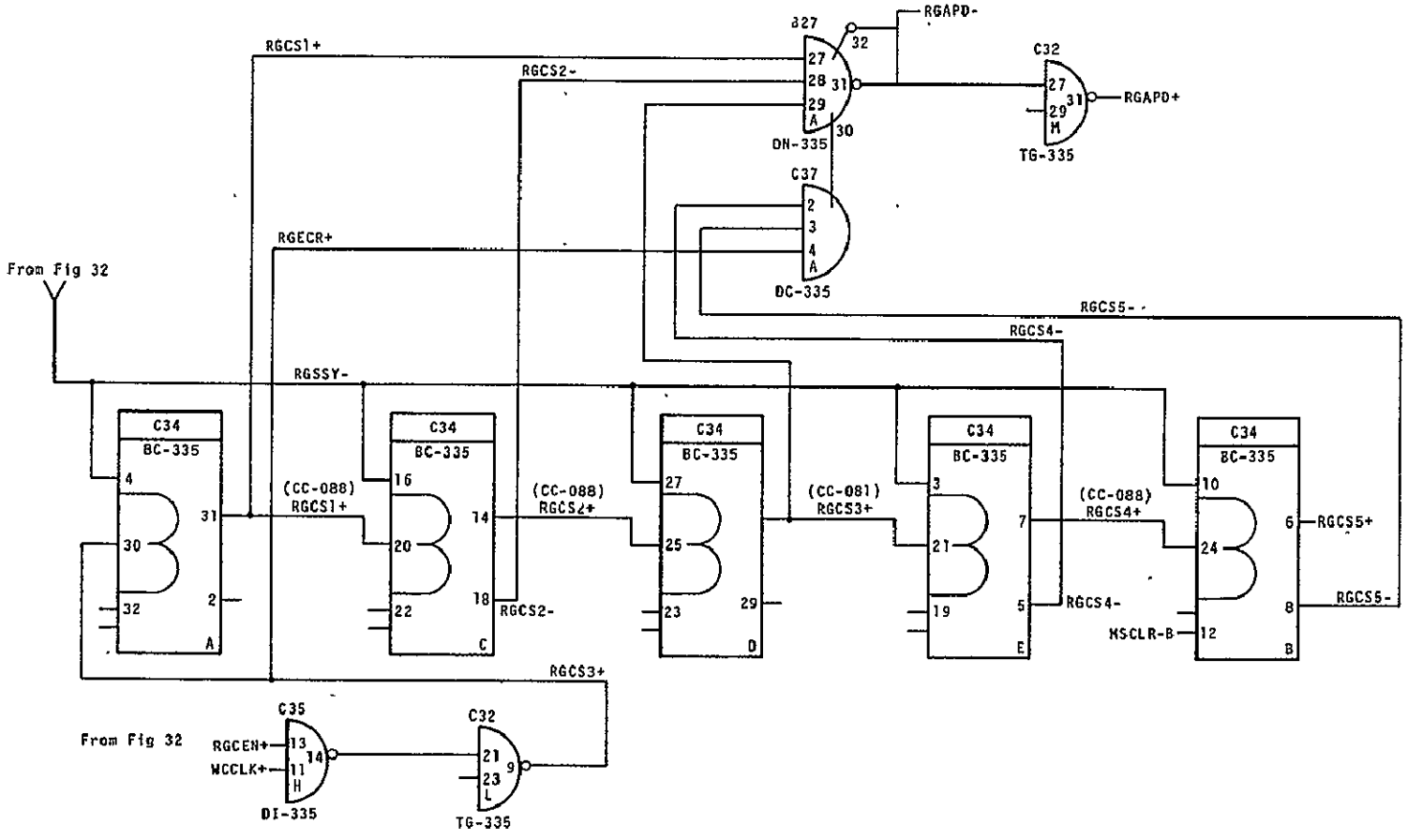


Figure 2-32. — Gap counter and record gap detection.

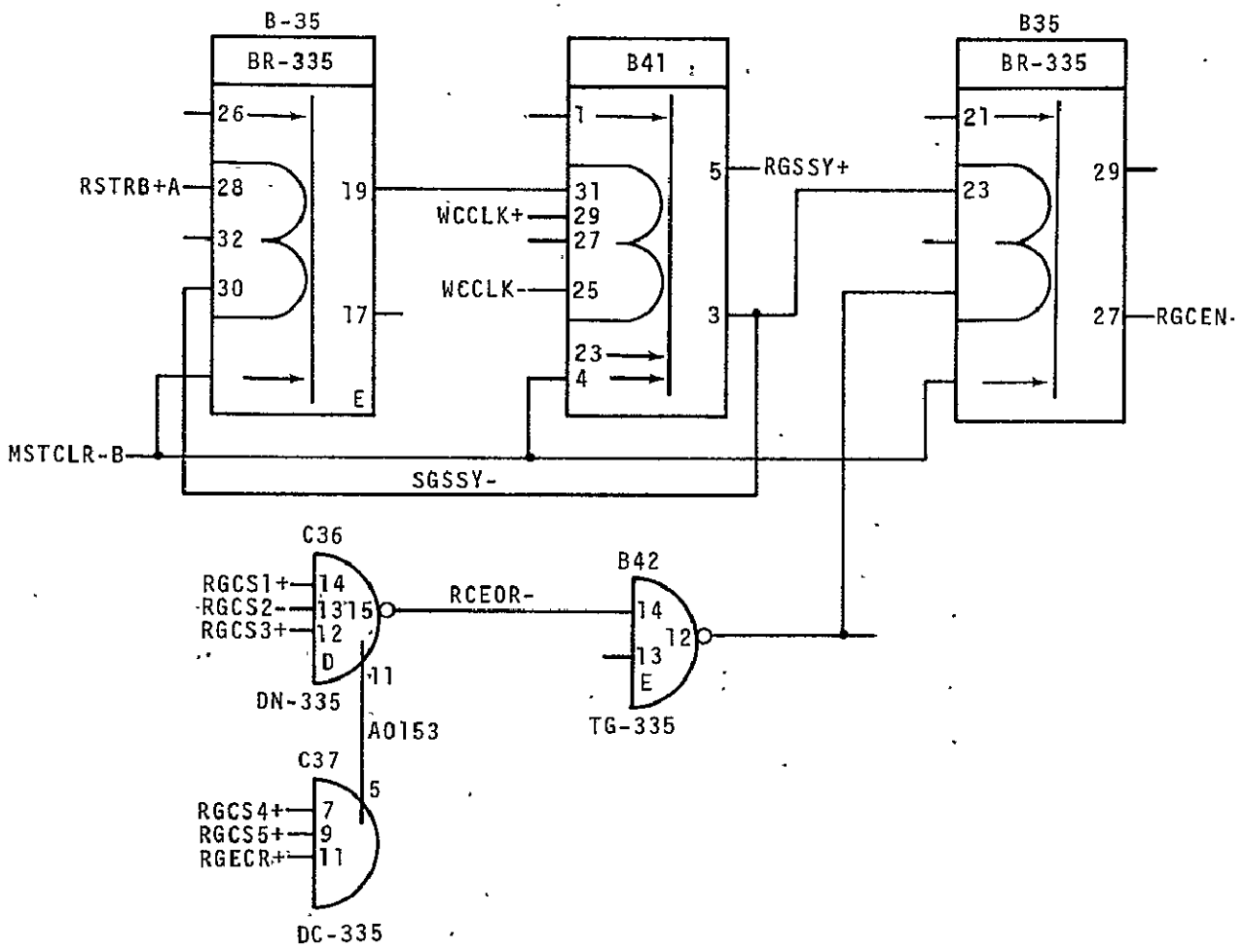


Figure 2-33. — Gap counter enable and read control end-of-record.

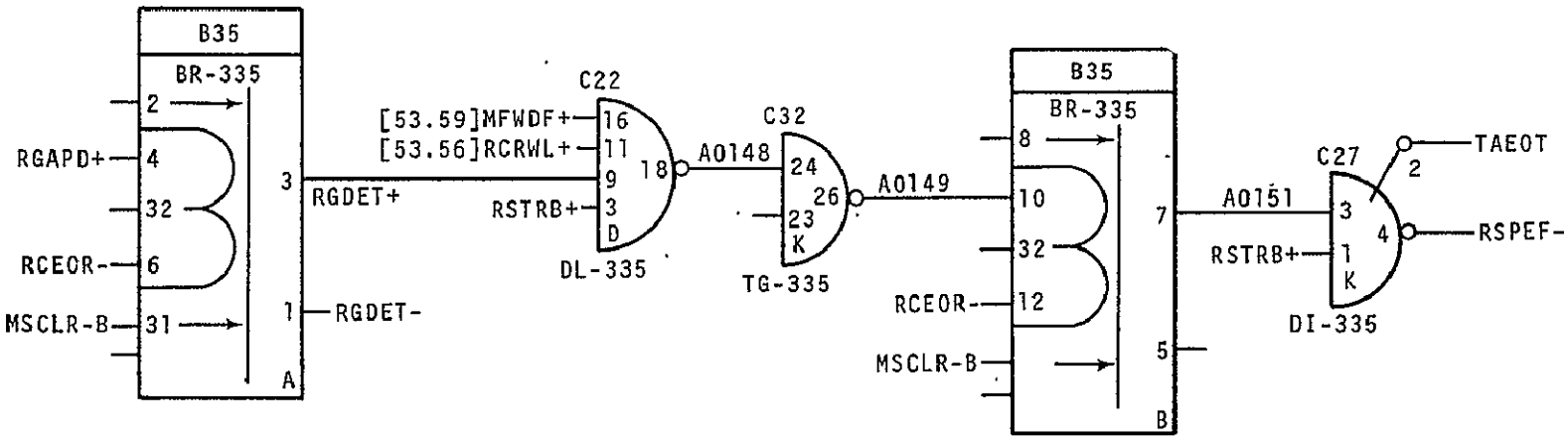


Figure 2-34. — No data gap detection

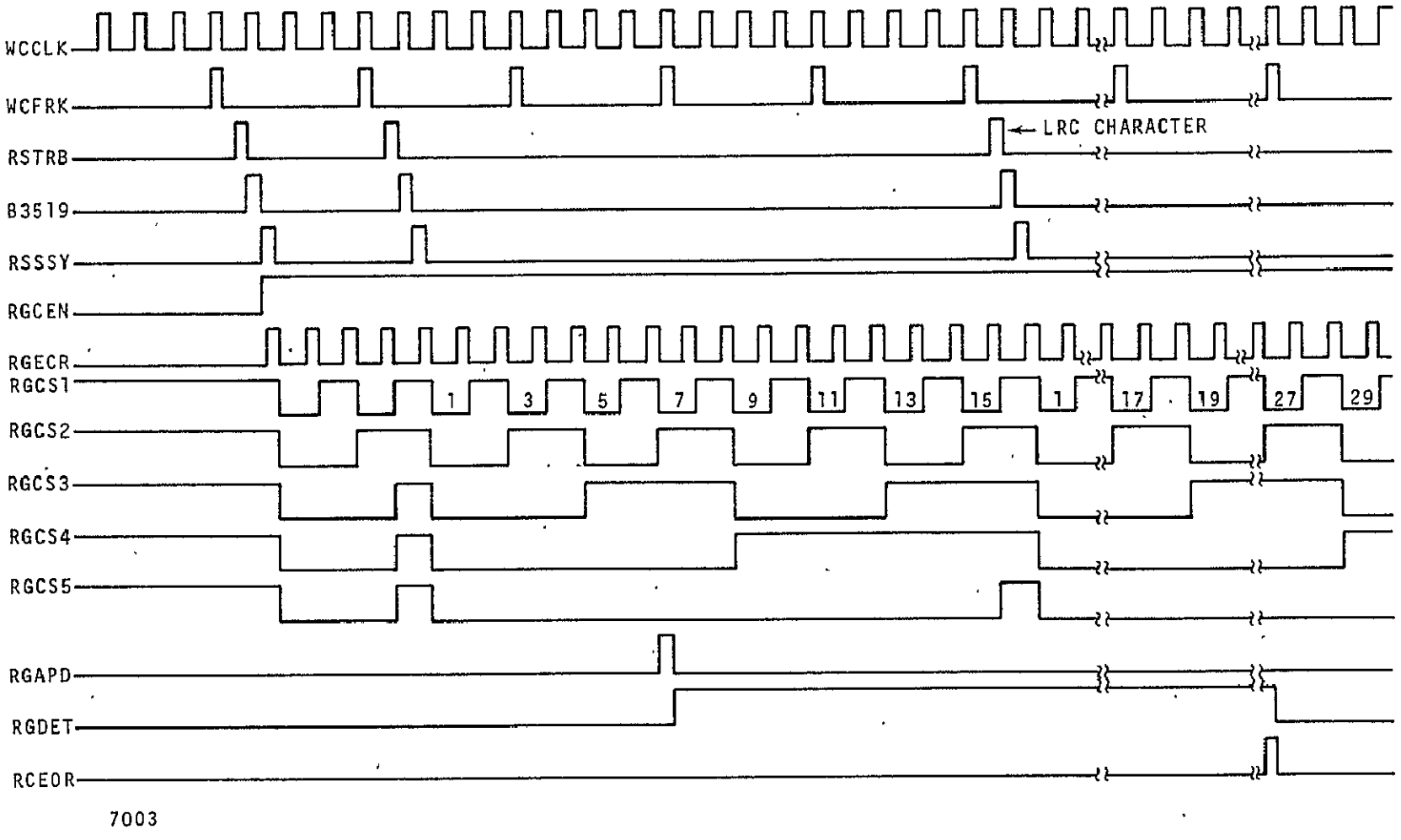


Figure 2-35. — Gap counter timing diagram.

2.3.4 WRITE CONTROL

The frequency of the write strobe pulses, the actual frequency of writing one's or zero's on the tape, is controlled by the density select switch on the selected MTT. This provides the two density select signals, STDR1+ and STDR2+ seen on figure 2-36. These signals allow either of two oscillators to control the timing of the TCU. If high density is selected then STDR2 is true and STDR1 is false. This gates the 230.4 kilohertz (kHz) oscillator signal from B22A through gate C32E to C35G. Because gate B25A has a ground on its input its output is always true. If a tri-density MTT had been used gate B25A would have been active. Flip-flop B26 is held set by STDR1 and its output is "and'ed" with the other signal at gate B25B. This forms signal WSCLK. This signal is divided by 2 by flip-flop B26C and its output is "and'ed" with WSCLK to form an output of B27B which is one-half the frequency of WSCLK but with the same pulse width. This signal (WCCLK-) is divided by 4 in flip-flops B26E and B26F. These outputs are "and'ed" with the input (WCCLK+ to form a signal WCFRK which is one-fourth the input frequency but with the same pulse width. This signal path has divided the input clock W800K by 8 but has preserved the pulse width. Thus WCFRK has a frequency of 230.4 kHz/8 = 28.8 kHz when the high frequency mode is selected. When the low density mode is selected the same division by 8 occurs but the low frequency clock starts at 320 kHz and is first divided by 2 in flip-flop B26A. This yields a frequency of 320 kHz/16 = 20 kHz when the low frequency mode is selected.

Whenever any write command has been issued by the CPU, flip-flop B34A (figure 2-37) will be set. This will trigger one of the two write oscillator delays one shot (B38A). This one shot will in turn trigger the other delay one shot (B38B). The purpose of this delay is to prevent any writing on the tape until tape motion has started and the correct inter-record gap has been formed. This signal (MWOD2+) goes through gate B37B, B37C to set

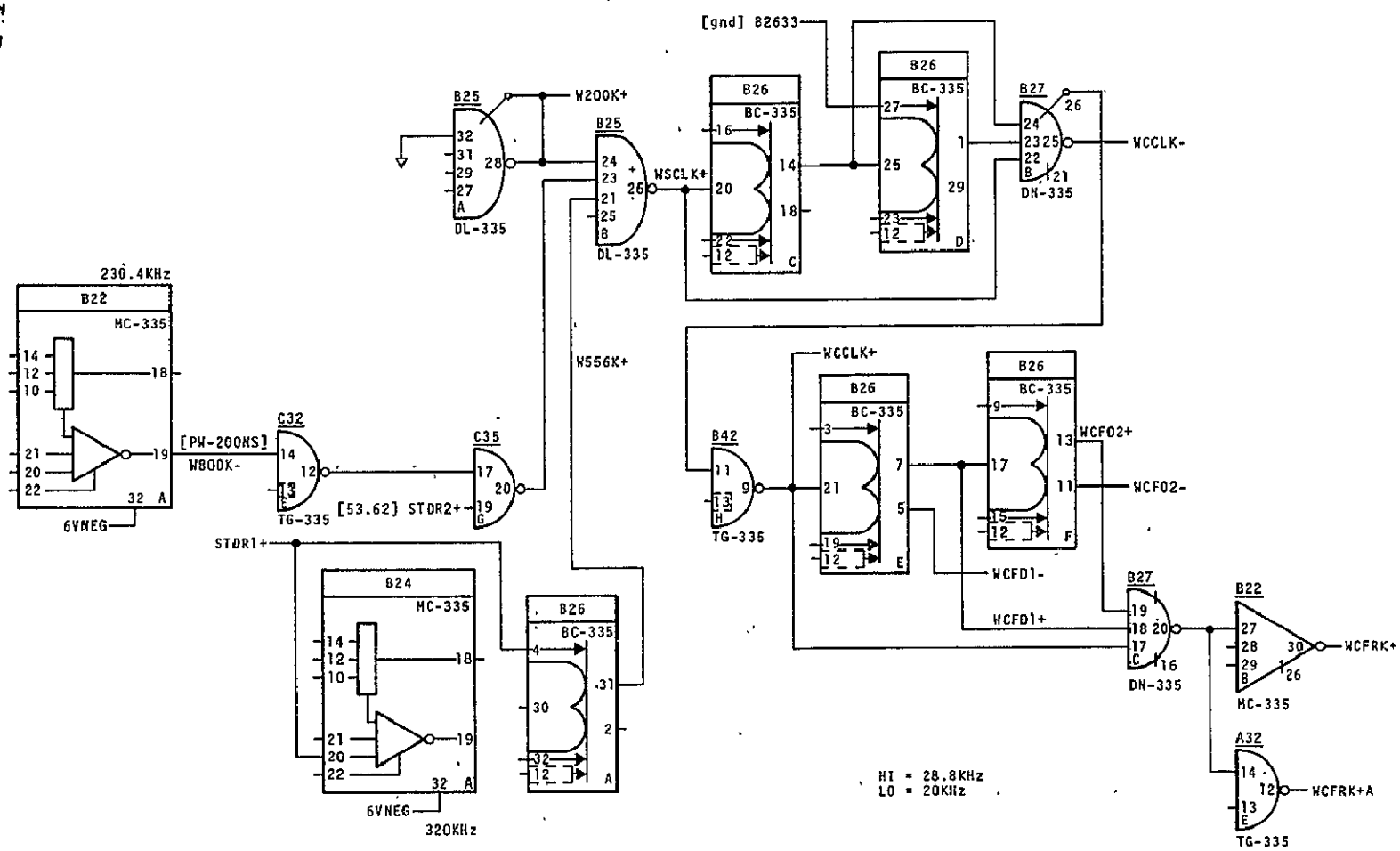


Figure 2-36. — Master oscillator, write clock, and frame clock.

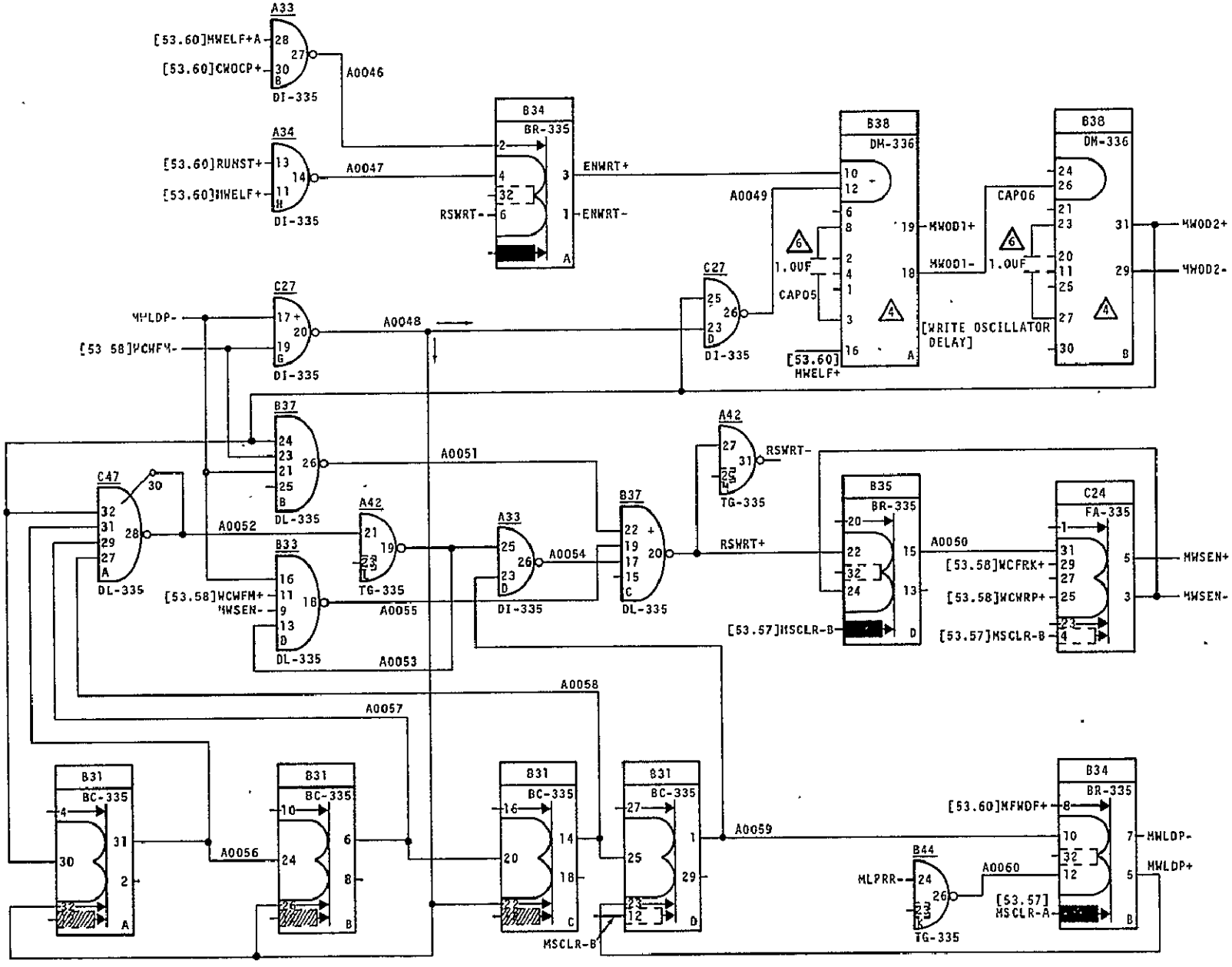


Figure 2-37. — Write oscillator delay.

flip-flop B35D. The output of B35D will set flip-flop C24C on the first clock pulse (WCFRK+). This flip-flop is the master write enable flip-flop and controls most of the writing operations.

If the MTT is positioned at the load point and a write command is issued, signal MWLOP will cause an additional delay of 16 oscillator delay times before MWSEN flip-flop will be set. This is to form the beginning of tape or load point gap of about 8 to 10 inches. Also if a write-a-file mark command had been issued, a delay of eight write oscillator delays would be generated before MWSEN flip-flop would be set. This is to form a 3- to 4-inch end-of-file gap. This circuitry is shown in figure 2-37.

During normal write operations a write-control normal write strobe (WCNWS) is generated by gates B25F and B44P (figure 2-38). If a write-file mark command is issued one file mark strobe pulse (WCFMS) will pass gate B25E. This will set flip-flop B34C and on the next write clock (WCFRK) a character count pulse will be generated (WCWST) from gate B25D. During other write operations the character count pulse is generated by B25C. After four character count pulses (WCWST), gate B27D (figure 2-39) will generate the write-reset pulse (WCWRP). The delay of four pulses was implemented by flip-flops B31F and B31E "and'ed" into gate B27D with the character count pulse. The output of B27D (WCWRP-) will reset B34C (figure 2-38) and allow one more write strobe pulse (WCFMS). The output of gate B27D will also go through inverter C32B (figure 2-39) and reset flip-flop B34D. Flip-flop B34D is used to store the write-file mark command until the task is complete.

2.3.5 MOTION CONTROL

Whenever a motion OCP is sent by the CPU, one or more motion control flip-flops are set. If an OCP which requires forward motion is sent then flip-flop C17B in figures 2-40 and 2-41 will

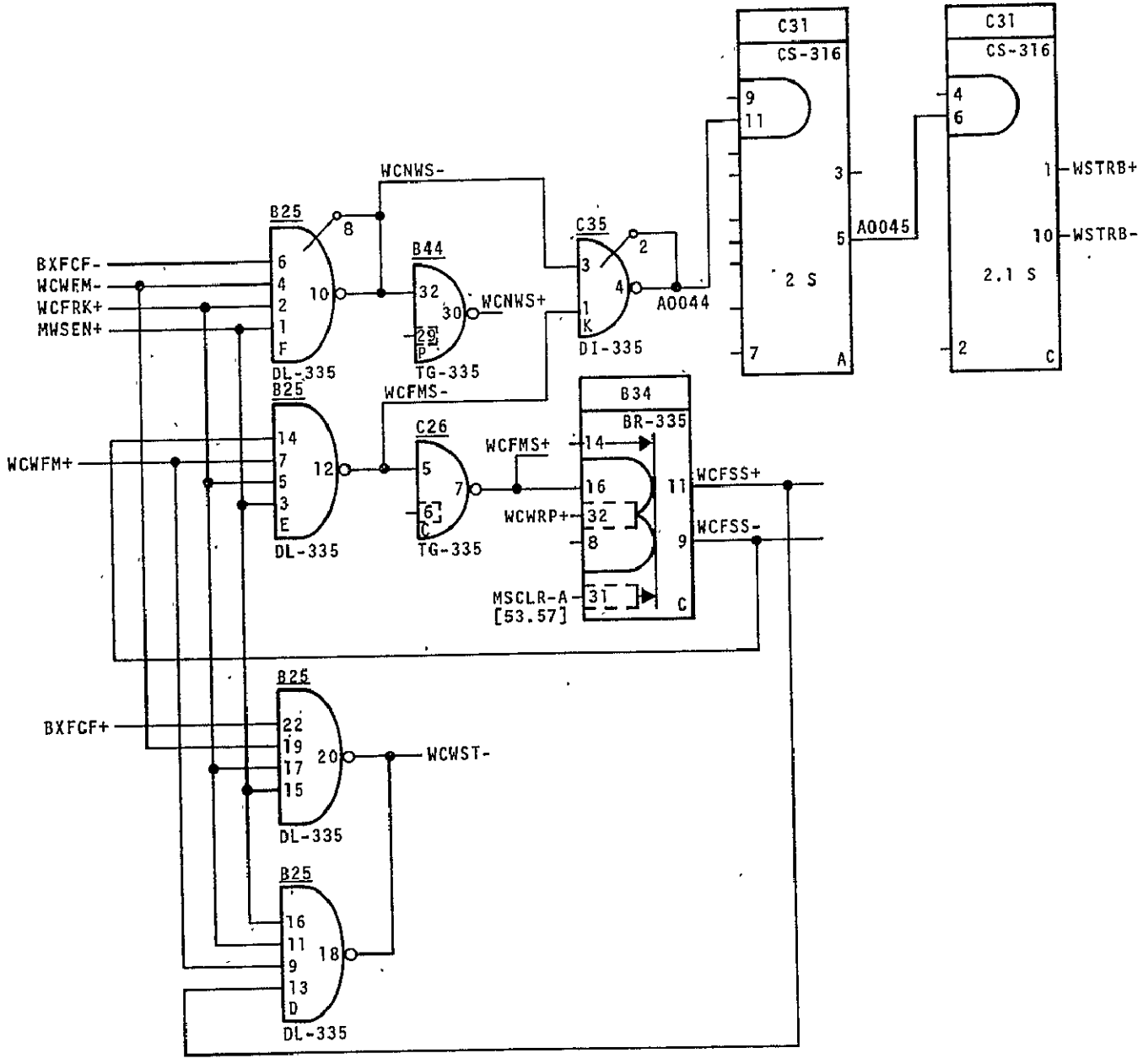


Figure 2-38. — Write strobe mode control.

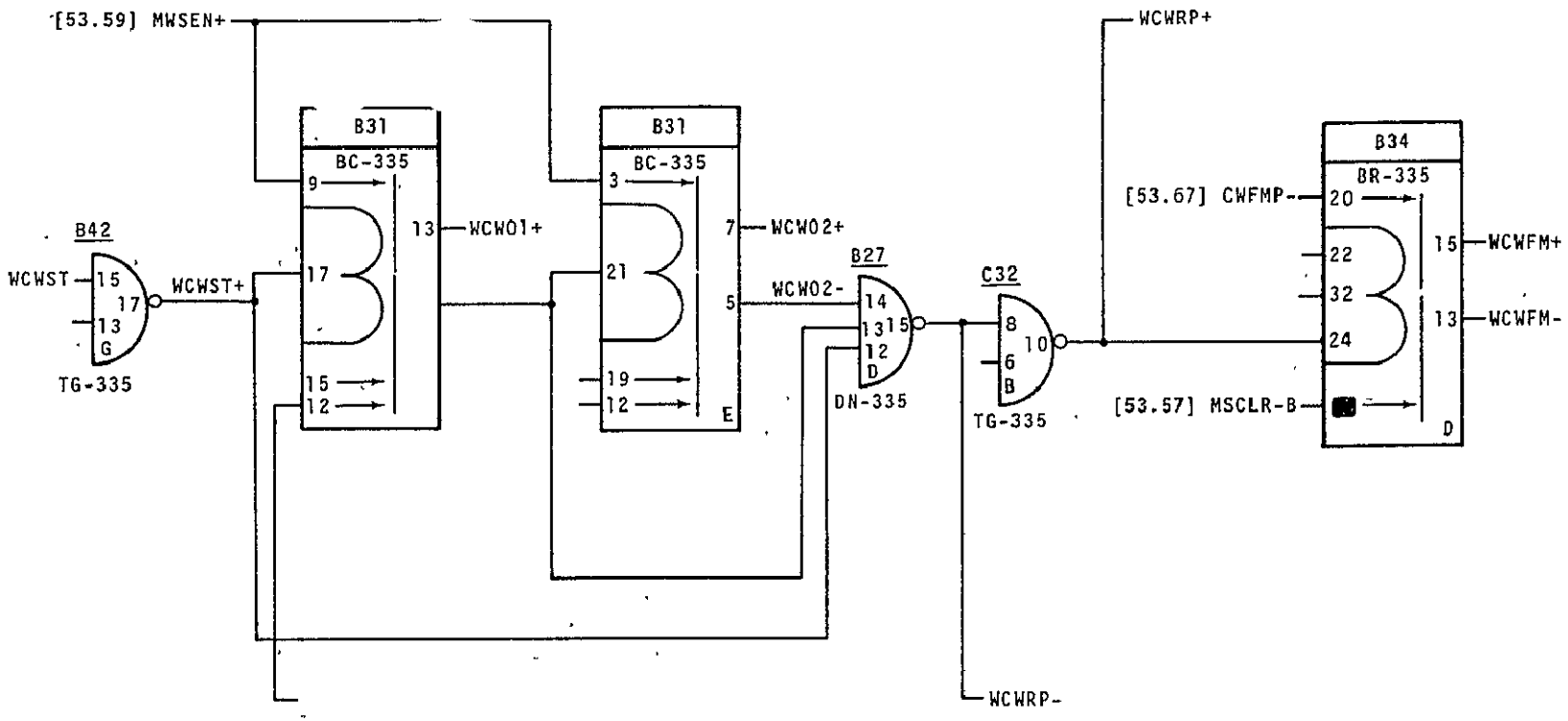


Figure 2-39. — Character count.

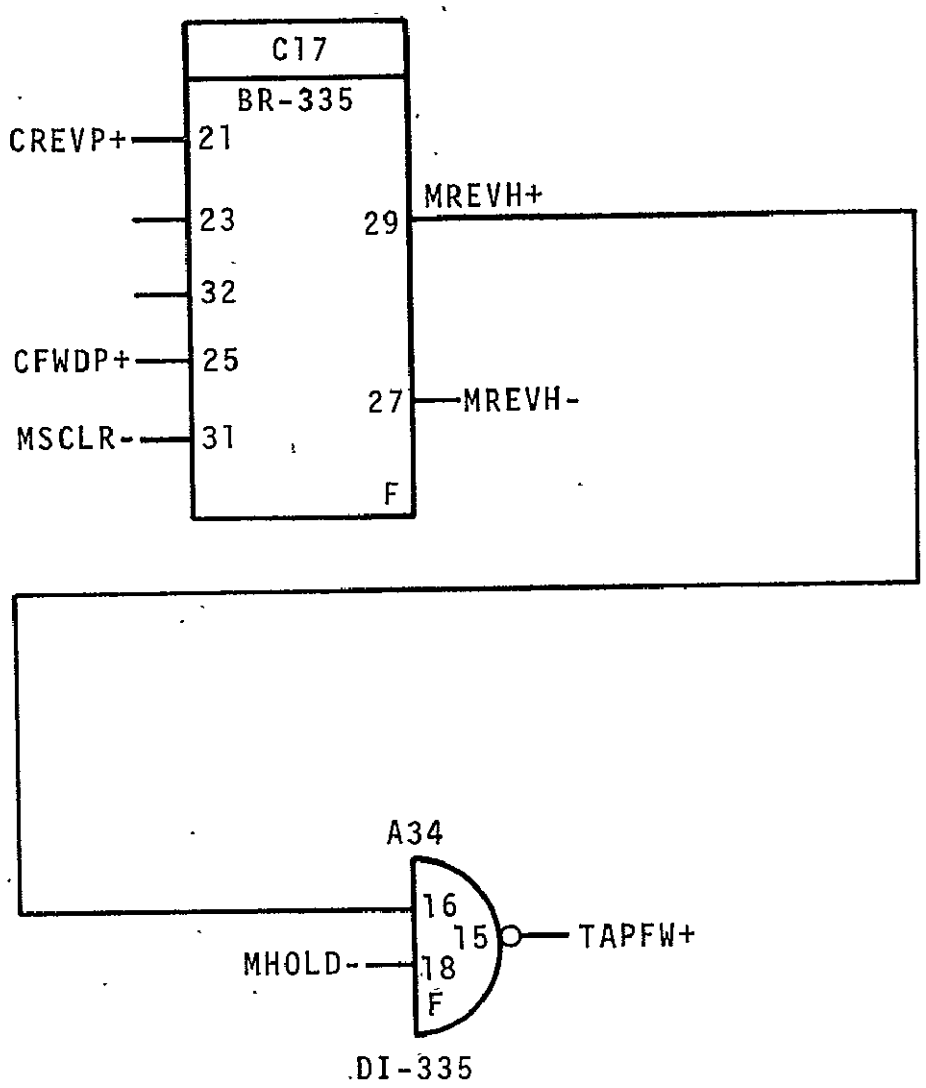
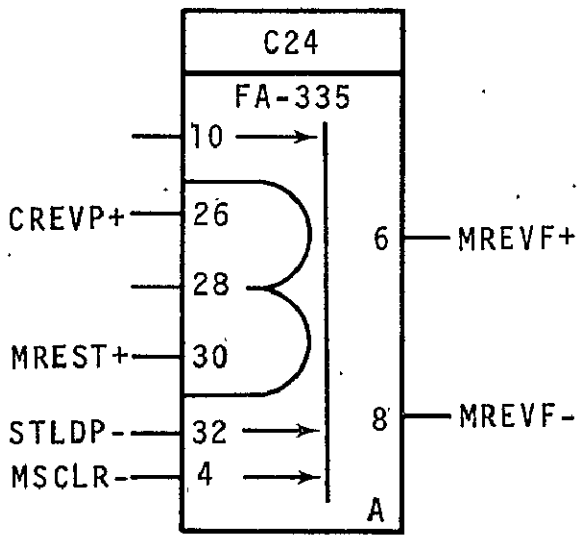
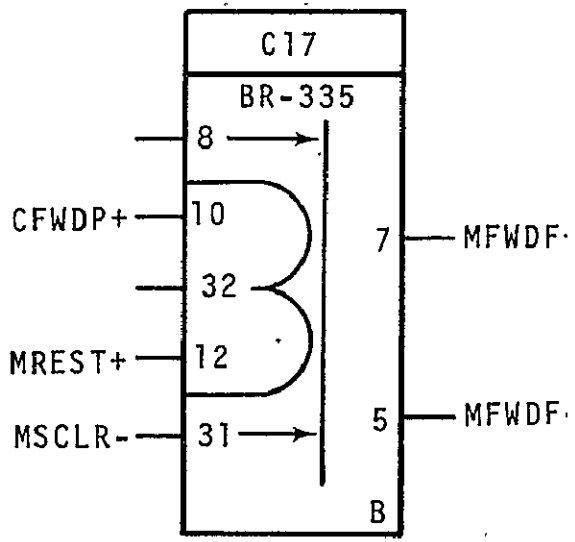


Figure 2-40. — Reverse motion history flip-flop.



Reverse Motion



Forward Motion

Figure 2-41. — Motion control flip-flops.

be set. This flip-flop will be reset by a master clear or by the motion reset (MREST) signal. If an OCP which required reverse motion had been sent then flip-flop C24A (figure 2-41) would be set. This flip-flop will be reset by the motion reset (MREST), by the master clear pulse, or by the selected MTT being at load point. Either of the two signals, motion forward (MFWDF) or motion reverse (MREVF), will enable setting the run/stop flip-flop C17C in figure 2-42. They will have held the DC (figure 2-43) set input low and thus kept RUNST- false. When the output of C35A (figure 2-42) goes positive it will enable the input to one shot (C18D). When motion hold (MHOLD-) and write hold (WHOLD-) are both positive, or go positive, one shot C18D will trigger and reset flip-flop C17C.

When a forward motion command (CFWDP+) is received flip-flop C17F (figure 2-40) will be reset, when a reverse motion command (CREVP+) is received the flip-flop will be set. This will generate MREVH. Signal MREVH is called the reverse motion history signal. It is used to control the motion-hold flip-flop B35C (figure 2-44). When the system busy signal (STBSY) is poitive the motion hold flip-flop will be reset if the reverse history signal (MREVH+) is positive and a forward motion is commanded (CFWDP+) or if the MREVH signal is not true (MREVH- is positive) and a reverse motion is commanded. The output of the flip-flop is used to inhibit motion if a change in tape direction is required.

The forward write extension (FWREX) one shot and the reverse extension one shot (REVEX) are triggered by the read control end-of-operation (RCEOP) signal depending upon the signal's (MWELF) master write enable flip-flop or the motion reverse flip-flop (MREVF). The outputs of the one shots are "or'ed" with the read extension pulse (figure 2-45) (READX), and the read control end-of-operations (RCEOP) signal from figure 2-31 to form the motion reset signal (MREST). This signal is used to reset

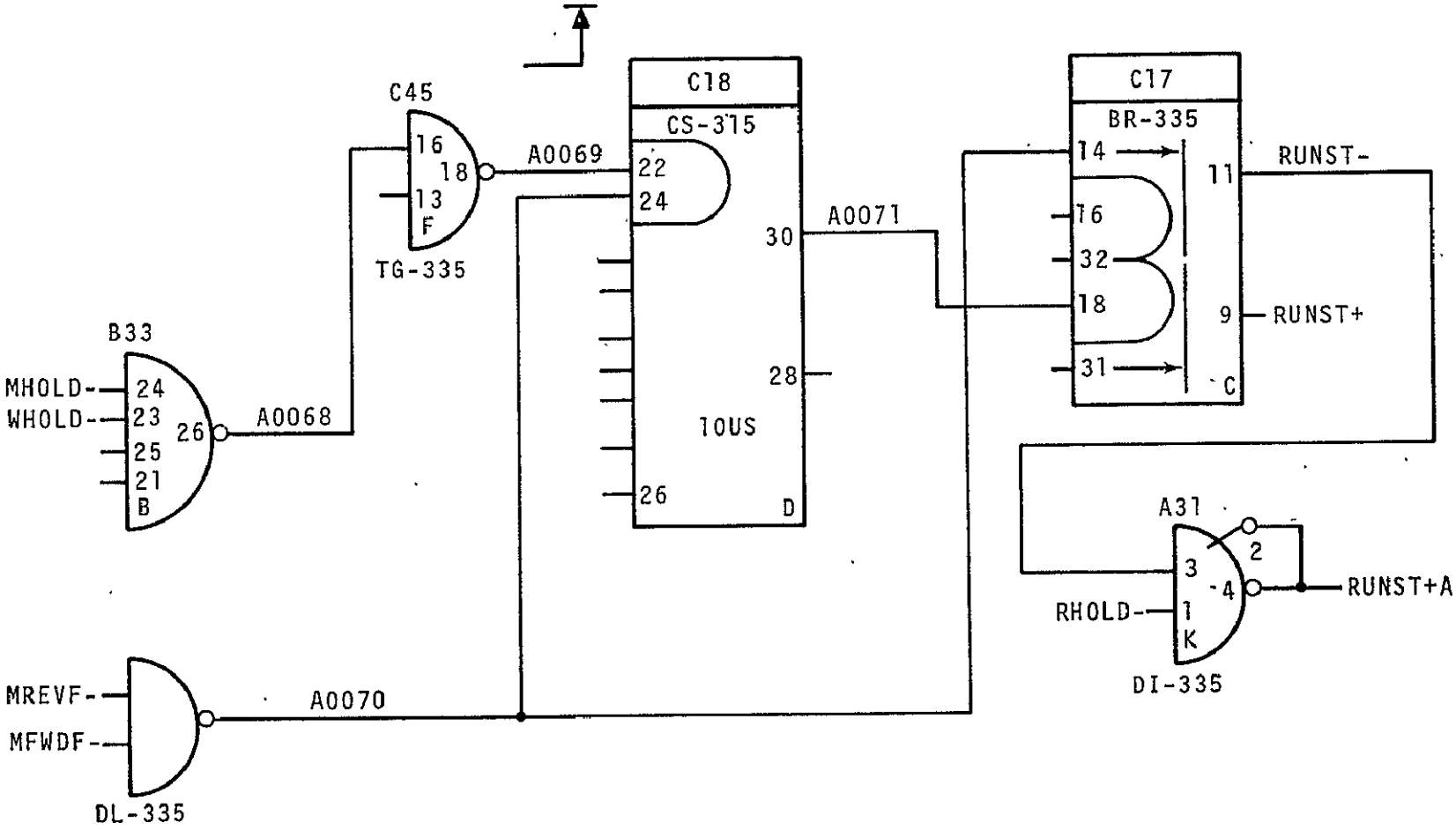


Figure 2-42. — Run/stop circuit.

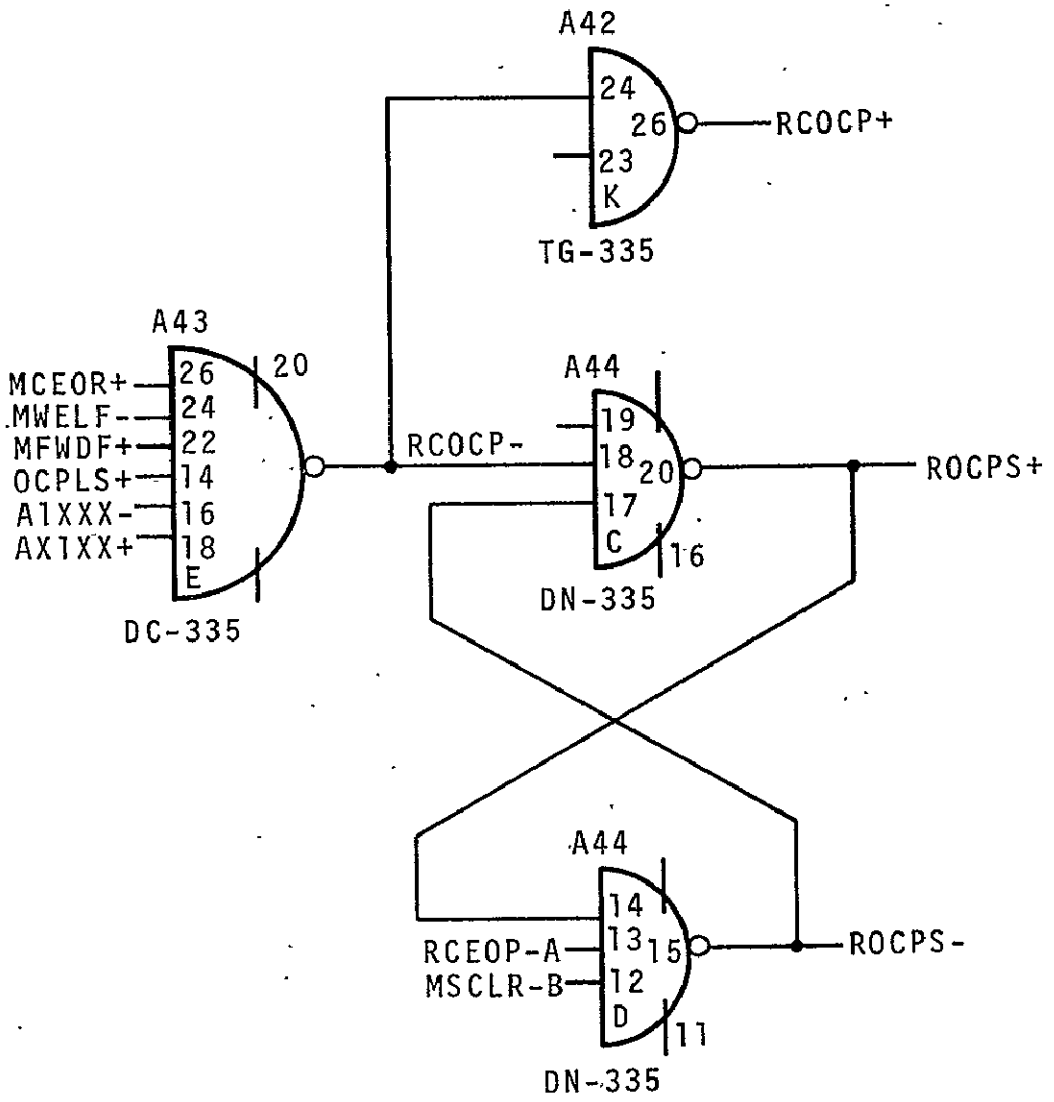


Figure 2-43. — Read OCP storage latch.

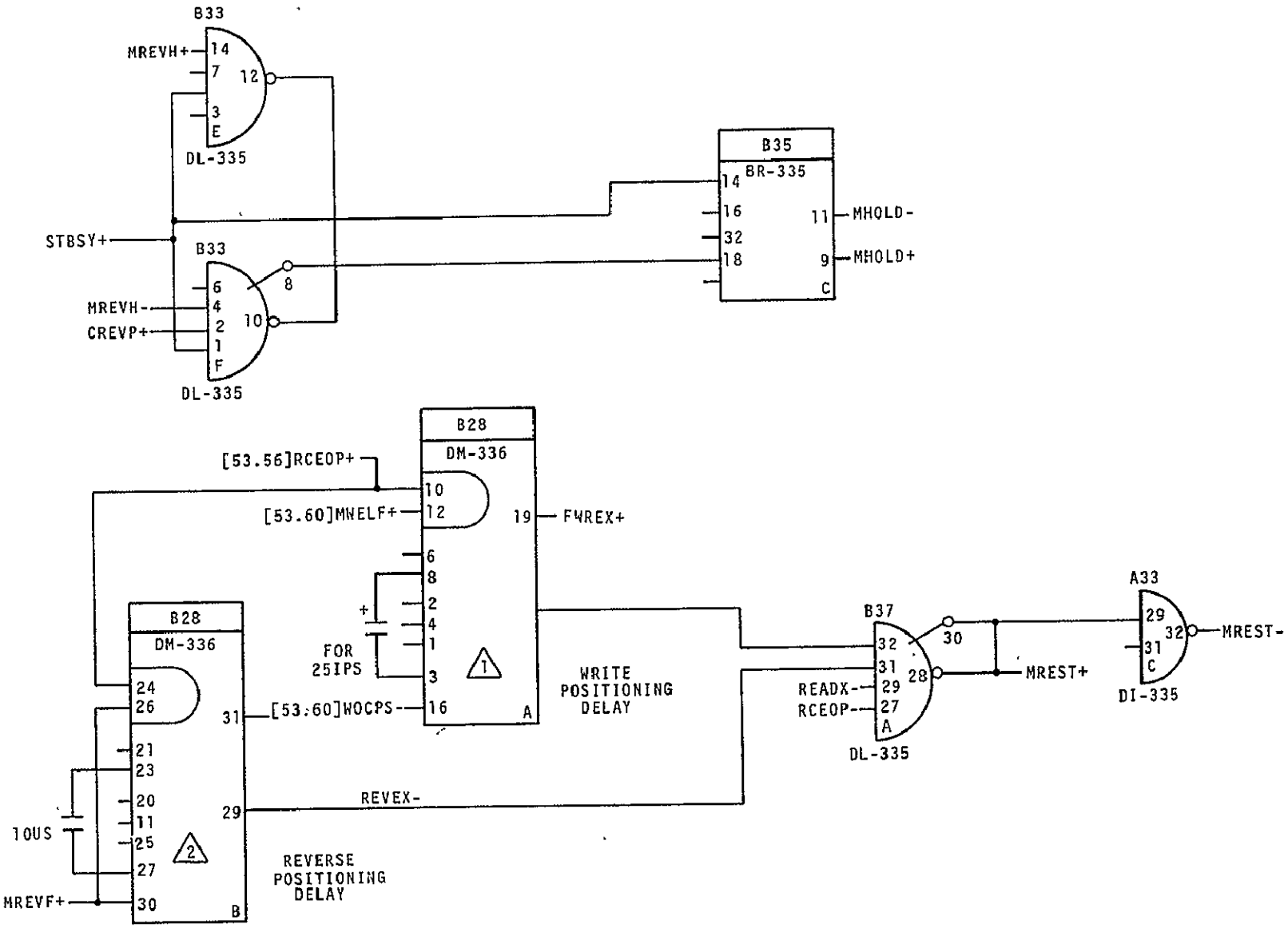


Figure 2-44. — Motion hold and motion reset circuits.

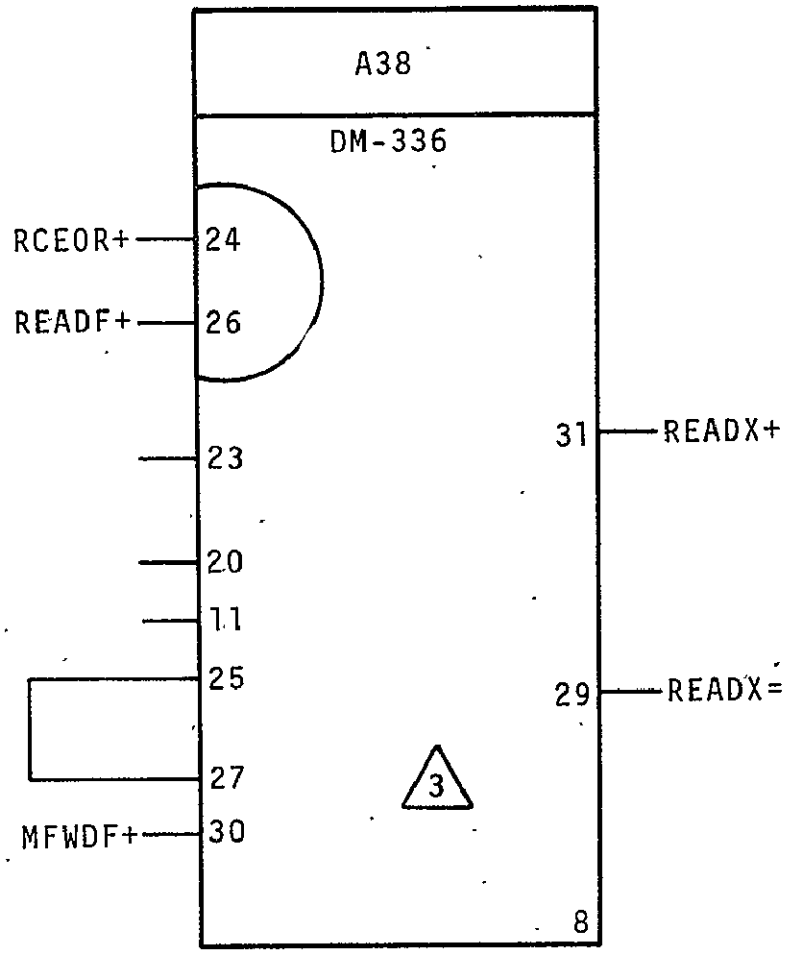


Figure 2-45.— Read extension one shot.

the motion flip-flops (figure 2-41). The motion flip-flops are reset on the trailing edge of the motion reset signal (MREST).

When the motion flip-flop is reset it will reset the run/stop flip-flop (see figure 2-42). This series of operations is shown in the timing diagram in figure 2-46. The forward write extension is used to form the proper inter-record gap and the reverse extension is used to position the read head correctly in the inter-record gap during reverse motion.

The read extension pulse (READX) is used to position the read head in the inter-record gap during any read function. (See figure 2-45.) During reverse read operations this one shot (A38B) is inhibited by the forward motion flip-flop (MFWDF) as shown in figure 2-41.

Any write OCP will cause the write enable flip-flop (C17A, figure 2-47) to be set if the selected tape transport (STBSY) is not busy. If STBSY is true (positive) the write enable flip-flop will not be set and the write hold flip-flop (C17D, figure 2-47) will be set.

2.3.6 MAGNETIC TAPE TRANSPORT SELECTION LOGIC

The tape control unit will handle four magnetic tape transports which are called tape unit A, B, C, and D. Figure 2-48 shows how the selected tape read bits are formed. If magnetic tape transport A had been selected signal SELTA+A would be true. This would gate the tape "A" read bits (TARB1) into the read bit bus. All the selected tape read bits (STRB1+) are wired "or" together. The signal is inverted and sent to the word-forming buffer where it is assembled into a 16-bit computer word. The signal at C35J (figure 2-48) tape "A" strobe bit (TASTB-) is also gated into the bus by SELTA+A signal to form the selected tape read strobe. Figure 2-49 shows a typical wired "or" read bit selection logic.

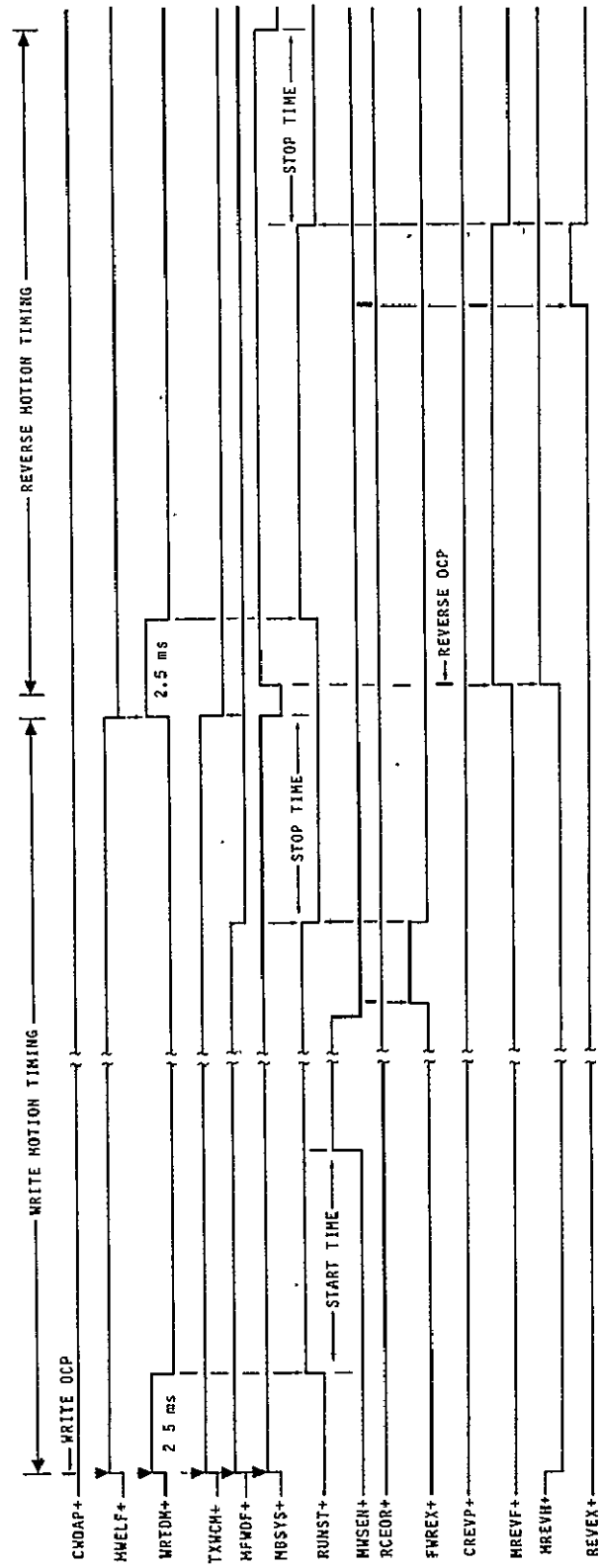


Figure 2-46. — Motion control timing diagram.

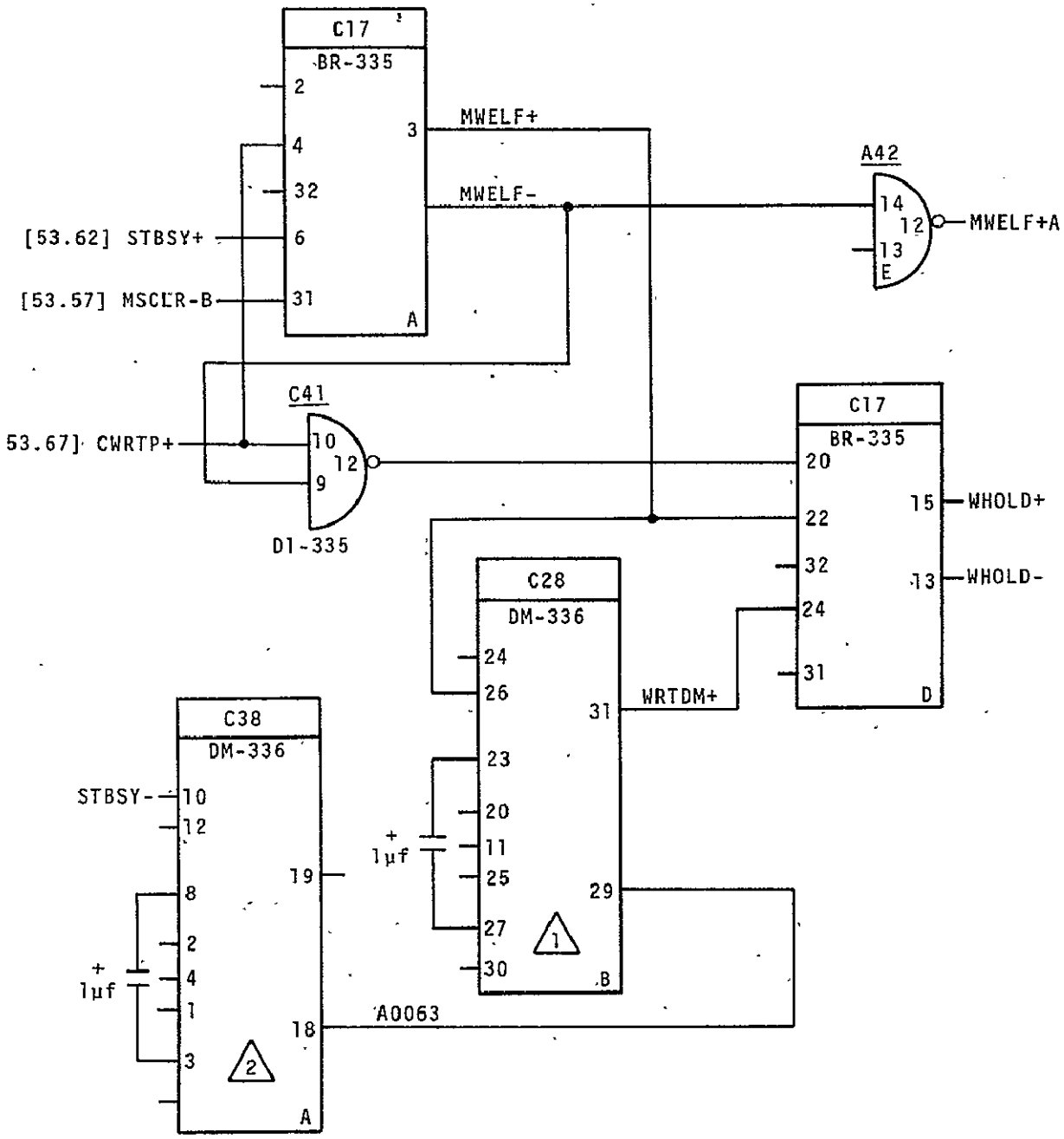


Figure 2-47. — Write enable flip-flop and write hold flip-flop.

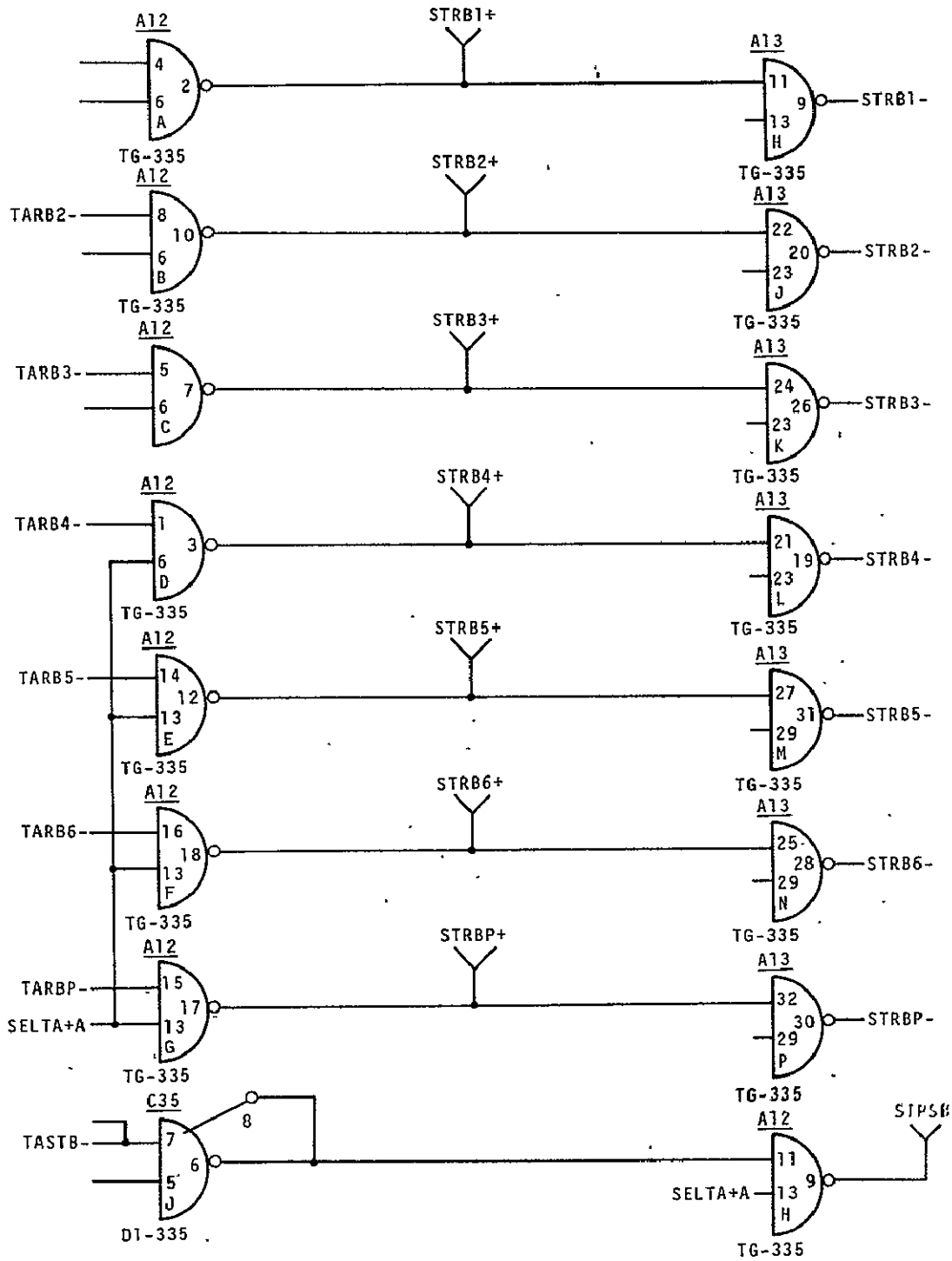


Figure 2-48. — MTT selection logic.

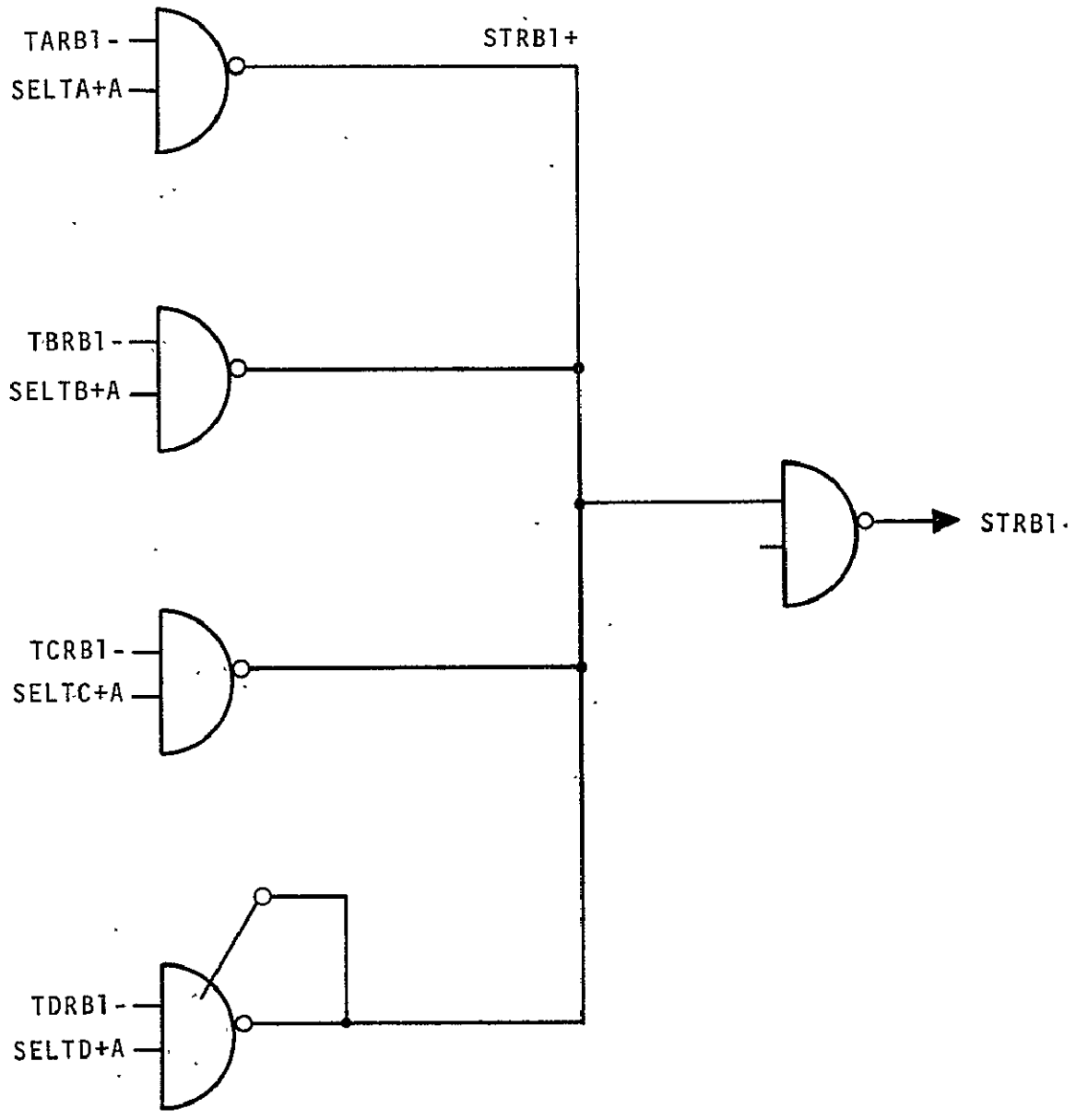


Figure 2-49. — Typical read bit selection logic.

During any forward or reverse motion of the MTT te selected tape busy status signal is generated. This is formed by a wired "or" bus on the input of gate A13F (figure 2-50). When the run/stop signal (RUNST+) and the select tape A signal (SELTA+) are true, gate A13B (figure 2-50) will set flip-flop A14C (figure 2-50). This will cause the selected tape busy status signal (STBSY+) to go true, gate A13F, (figure 2-50). When the output of gate A13B goes plus it will trigger one shot C28A. After 12 milliseconds the output of the one shot will reset flip-flop A14C. This will cause the selectd tape busy status signal to go false.

Figure 2-51 contains the remaining tape "A" selection logic. Gates B43A, B43G, B43H, and A21A form the select tape "A" latch (SELTA). The output of the latch is used to gate the selection-logic signals into the correct selected signal bus. Also shown in figure 2-51 is the selected tape at load point (STLDP), selected tape density (STDR1 and STDR2), rewind logic (REWID). Gate A41H forms the selected tape ready signal (SREDY-). The signal formed in gate A33K (SRWDS-) selected tape rewind status is used to tell the CPU that the selected tape is rewinding when the CPU checks its status by a SKS instruction. Also the signal generated in gate A41G (SWPER+) is used to tell the CPU that the selected tape has been enabled to write, that is, a write ring has been mounted on the tape roll.

The end-of-tape flip-flop B34E is shown in figure 2-52. This flip-flop is set whenever the selected tape unit reaches the end-of-tape marker. All the tape units are wired "or" to the selected tape end-of-tape bus (STEOT-). This flip-flop is reset by the selected tape load point signal (STLDP-) which comes from gate B44B (figure 2-51).

Only the selection logic for magnetic tape transport "A" has been shown, but the other three MTT selection logics are similar in operation.

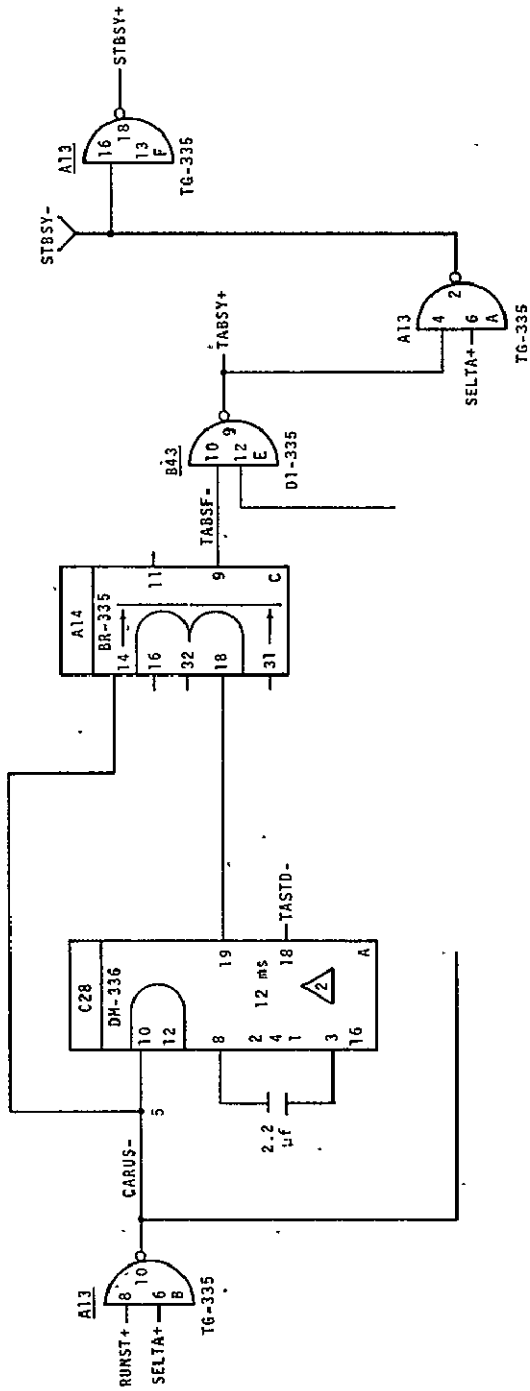


Figure 2-50. — Selected tape busy selection logic.

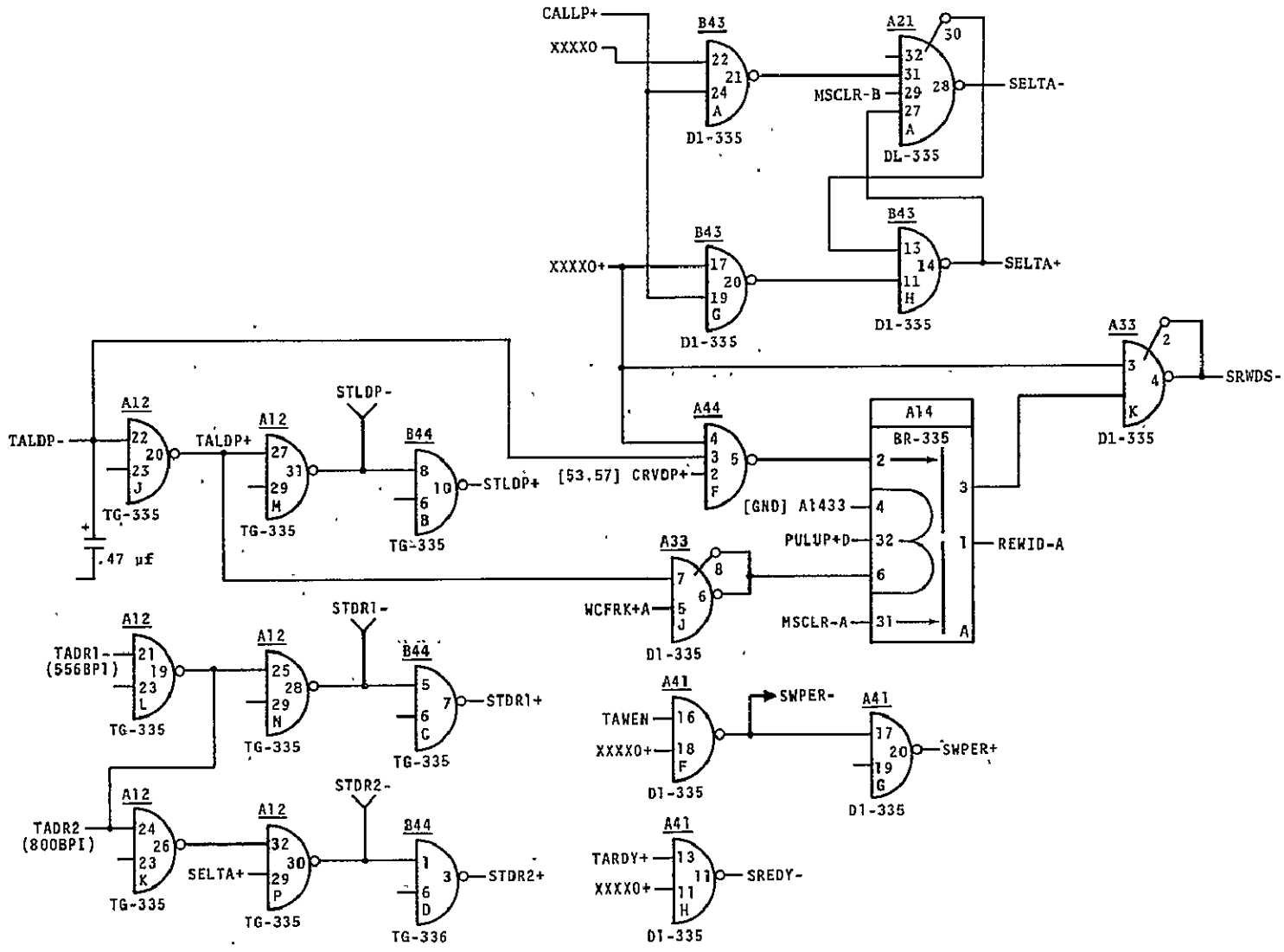


Figure 2-51. — Selection logic.

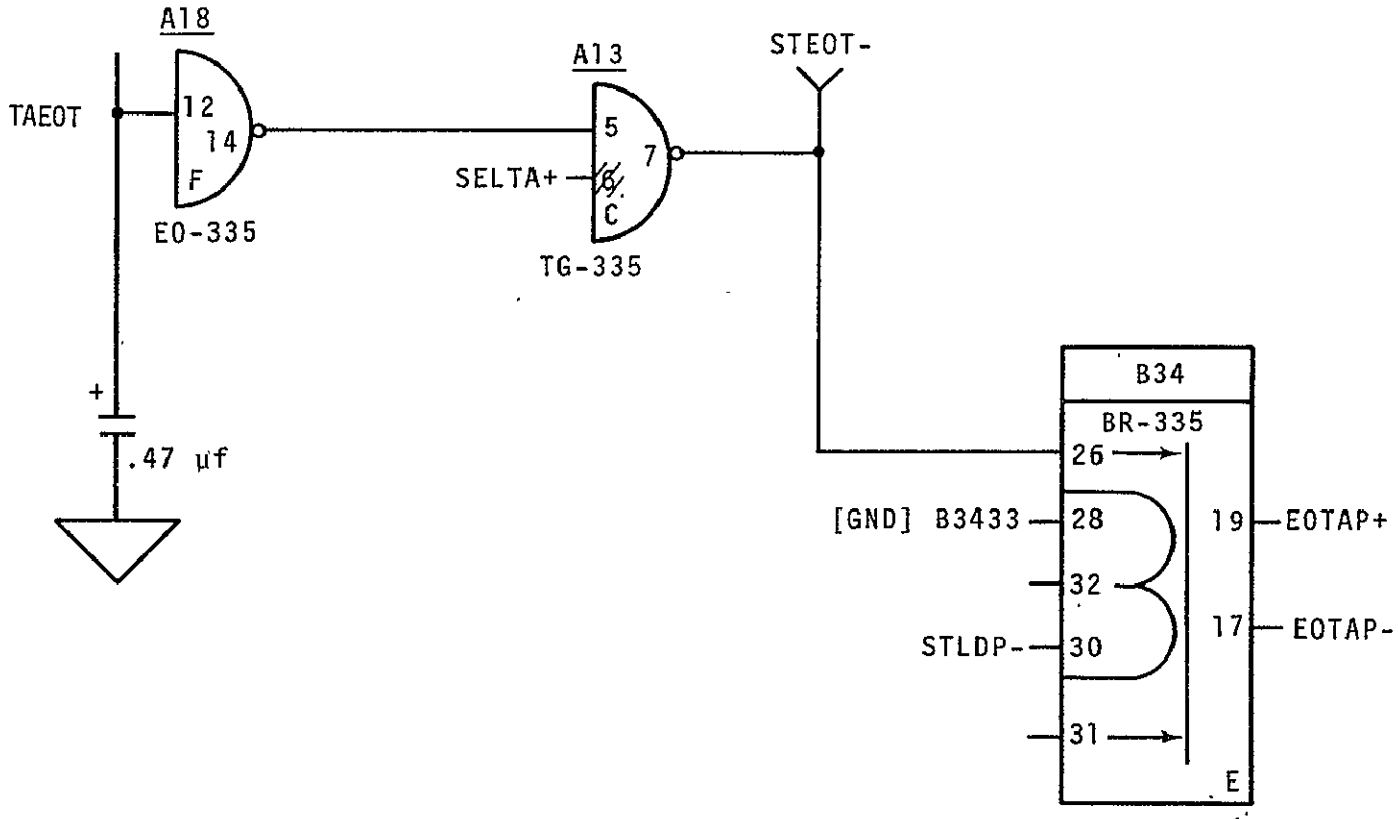


Figure 2-52. — End-of-tape logic.

2.3.7 MAGNETIC TAPE TRANSPORT DRIVER LOGIC

The MTT driver logic consist of a number of line driver amplifier packs (Honeywell CC-010) which are capable of driving up to 100 feet of twisted pair cable. The data lines, WDAT1 through WDATP (figure 2-53), are the seven signals which are sent one to each track of the MTT (table II).

The control signals, run/stop (TARUS), forward/reverse (TAFWD), write strobe (TAWST), and rewind (TARWD) are shown in figure 2-54. Figure 2-55 shows the last two command signals to the MTT. The write reset pulse generated by the one shot C18B is used to reset the character flip-flop in the MTT. This is the longitudinal parity bit which is written on the tape.

2.3.8 DIRECT MULTIPLEX CONTROL (DMC)

Direct Multiplex Control operation is started by the CPU issuing a DMC command to the TCU. If a set DMC mode normal command is issued the DMC status latch (figure 2-56) will be set by the signal set DMC normal (SDMCN-) which is formed in gate A55A by "and'ing" AX3XX+ and AOCPO+. This signal (SDMCN-) also resets the DMC auto mode flip-flop if it is set (A53D, figure 2-57). If a DMC auto mode command had been sent by the CPU the DMC mode latch would have been set and the DMC auto flip-flop would have also been set.

After the DMC mode has been set the TCU will issue a data interrupt line signal (DILXX+) to the DMC when the TCU has data ready or requires data from the CPU. Because the TCU DMC interface has the auto channel option, two DILXX lines are required. These signals are generated by gates A54B, A55K (DILXX+A) and A54C, A55J (DILXX+B) shown in figure 2-58.

During normal DMC read operations gate A57G (figure 2-58) will detect an end-of-operation (RCEOP+) and will generate EXSTP-. This signal will set flip-flop A53B (figure 2-57). This

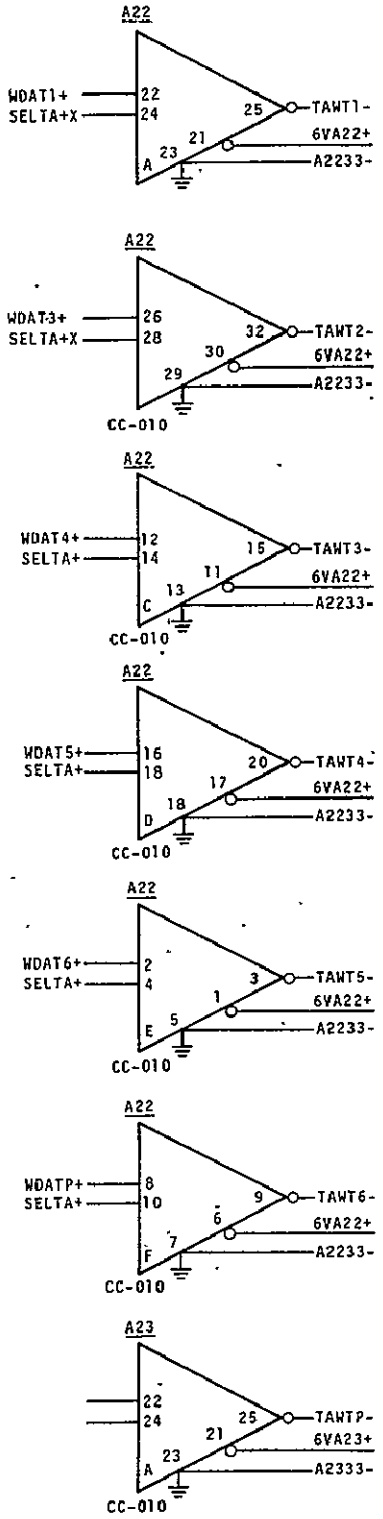


Figure 2-53. — Tape "A" driver logic (write bits).

TABLE II.- SIGNAL NAME

Table II contains the mnemoric index for the seven-track MTT.

MNEMONIC INDEX

Signal	LBD No./Source	Definition
OCPLS	5366K4	Output control pulse
OTBxx	5350XX	Output transfer bus, bits 1 through 16
INBxx	5351XX	Input transfer bus, bits 1 through 16
AOCP0	5366K7	OCP and address bit 7 (7 = 0)
AOCP1	5366L3	OCP and address bit 7 (7 = 1)
A1XXX	5366C1C	Address bit 7 = ONE (+) or ZERO (-)
A3V7X	5366G6	Address 3 or 7
ACKAX	DMA	Acknowledge from DMA
ADBxx	5369XX	Address bus, bits 7 through 16
AXxXX	5366JX	Decode function bits
B2CPW	5353B3	Buffer two characters per word
BCH3T	5353E1	Buffer character three times
BCHDx	5353X3	Buffer character distributor 1 through 3
BCLCT	5353E3	Buffer control last character time
BCOCS	5353G7	Buffer control, odd character strobe
BCRDY	5353F1C	Buffer control ready
BCRES	5353K6	Buffer control reset
BCSCx	5353K1C	Buffer control strobe character 1 through 3
BEINB	5353C5	Buffer enable input bus
BTTOE	5353K8	Buffer transfer output bus enabled
BWDBx	5353JX	Buffer write data, bits 1 through 6
BXFCF	5353G8	Buffer transfer control flip-flop
BSFER	5353H6	Buffer transfer
CALLP	5366K8	Any OCP (housekeeping pulse)
CEVEN	5354D1C	Even parity

TABLE II.- SIGNAL NAME (Continued)

Signal	LBD No./Source	Definition
CEVPP	5367B8	Even parity OCP
CFWDP	5367E5	Forward OCP
CHANB	5361G3	Autoswitch subchannel B
CHENX	5361B9	Channel enable from DMA
CHSLI	5361C7	Channel select
CHSLX	5361B7	Channel select from DMA
CMKXX	5372	Clear mask flip-flop
CREVP	5367E8	Reverse OCP
CRINT	5367D2	Control ready interrupt
CRTEP	5367B6	Read OCP
CRWDP	5367E9	Rewind OCP
CSFMP	5367B2	Search file OCP
CW3BY	5367B11	Write three binary OCP
CWDAP	5367D2	Write data OCP
CWFMP	5367E11	Write file mark OCP
CWOCP	5360F7	Continuous write OCP pulse
CWRDP	5367D7	Write or read data OCP
CWRTP	5367D4	Write OCP
CxRUS	5362G1	Selected transport run/stop
DACKR	5361B11	Data acknowledge ready
DALXX	5361B4	Device address lines from DMC
DAUTO	5361G9	Autoswitch mode
DERLF	5361G7	End of range flip-flop
DERLX	5361D5	End of range
DILXX	5361K1/K4	Data interrupt lines to DMC
DMCAD	5361C4	DMC address
DMCMF	5361E1	DMC mode flip-flop
DMRES	5361E4	DMC subchannel reset
DRLIN	5367L5	Data request line
EOTAP	5362G6	End of tape storage
ENDXM	5361L7	End of transmission

TABLE II.- SIGNAL NAME (Continued)

Signal	LBD No./Source	Definition
ENWRT	5359D5	Enable write oscillator delay
ERLXX	5369F5/F10	End of range
EXSPF	5361G5	External stop flip-flop
EXSTP	5361H11	DMA/DMC external stop
FMPLS	5356B9	File mark pulse
FWREX	5359C1	Forward write extension
LATPE	5356F2	Lateral parity error
LATPS	5356H4	Lateral Parity Flip-Flop Strobe
LCT2C	5353D1	Buffer character two time
MSBYS	5359L2	Motion busy status
MCEOR	5360A10	Motion control, end of record
MFWDF	5360M7	Motion forward flip-flop
MHOLD	5359J3	Motion hold
MLPRR	5359L1	Motion control, load point set pulse
MREST	535904	Motion reset
MREVF	5360P9	Motion reverse flip-flop
MREVH	5360L10	Motion reverse history
MSCLR	5357K6	Master clear
MSTCL	5372D5/D10	Master clear
MTINT	5367H3/H8	Magnetic tape interrupt
MTADD	5366C3	Magnetic tape address
MTMSK	5367L10	Magnetic tape mask
MWELF	5359K5	Write enable flip-flop
MWLDP	5359H10	Write at load point
MWOD2	5359G6	Write oscillator delay DM No. 2
MWSEN	5359H8	Write strobe enable
PIL00	5367L8	Program interrupt line
PULUP		Pull-up runs for unused flip-flop dc inputs
PWRFL	5369D4/D9	Power fail
ROL12	5355D1	Read octal twelve
R1Bxx	5350xx	Rank 1, bits 1 through 16

TABLE II.- SIGNAL NAME (Continued)

Signal	LBD No./Source	Definition
2Bxx	5350xx	Rank 2, bits 1 through 16
RCDIP	5356L1	Read control drop-in pulse
RCEOF	5356G11	Read control end of file
RCEOP	5356L11	Read control end of operation
RCEOR	5357L5	Read control end of record
RCFMD	5356D8	Read control file mark detected
RCPEF	5356K8	Read control parity error flip-flop
RCRWL	5356L6	Read control read or write level
RCSFM	5356J11	Read control search file mark
RDPMT	6354L8	Read permit
READF	5356K4	Read flip-flop
READX	5359E2	Read extension pulse
REDMC	5361B3	Reset DMC OCP
RESR1	5353F11/J6	Reset rank 1
REVEX	5359A2	Reverse extension
RGAPD	5357L2	Gap detect pulse
RGCEN	5357H2	Gap counter enable
RGCSx	5357X10	Gap counter stage 1 through 5
RGDET	5357B5	Gap detected flip-flop
RGECR	5357C10	Gap counter enable clock
RGSSY	5357F1	Gap counter set synchronized
RHOLD	5360E11	Run hold
ROCPS	5360G5	Read OCP storage
RRLIN	536904/D10	Reset ready line
RRLAD	5353C11	Reset ready line and address
RRLAX	5353B9	Reset ready line and address
RSPEF	5355	Set parity error flip-flop
RSTRB	5357C2	Read strobe
RSWRT	5359E9	Reset write oscillator delay
RUNST	5360J2	Run stop control level
RWIND	5362	Rewind busy flip-flop
RWOCP	5360C8	Read/write OCP

TABLE II.- SIGNAL NAME (Continued)

Signal	LBD No./Source	Definition
RWWIN	5367F2	Read/write window
SDMCA	5361B2	Set DMC auto OCP
SDMCN	5361B1	Set DMC normal OCP
SELTX	5362L1	Select MTT X
SMK01	5367J10	Set mask
SMKXX	5372 F4/F9	Set mask general output strobe
SREDY	5362	Selected transport ready (drive operational)
STBSY	5362L1	Selected transport busy
STEOT	5362D10	Selected end of tape
STDRx	5362F9	Selected transport density status
STLDP	5362D11	Selected load point
STRBX	5355XX	Selected read bits 1 through 7
STRBP	5362B9	Selected read parity bit
STRSB	5362C10	Selected transport read strobe
TAPFW	5360F11	Tape forward control
TRWID	5360P6	Transport rewind pulse
TxBSF	5362J1	Transport x busy flip-flop
TxBSY	5362K1	Transport x busy
TxDR1	5372xx	Transport x density status
TxDR2		
TxEOT	5372xx	Transport x, end of tape
TxFWD	5370Jx	Transport x, forward/reverse
TxLDP	5372xx	Transport x, load point status
TxRBx	5372xx	Transport x, read bit x
TxRDY	5372xx	Transport x, ready (operational)
TxRUS	5368Cx	Transport x, run/stop command
TxRWD	5368Cx	Transport x, rewind command pulse
	5369Cx	
TxSEL	5372xx	Transport x, selected (read permit)
TxSTB	5372xx	Transport x, read strobes
TxSTD	5362H1	Transport x, stop time delay

TABLE II.- SIGNAL NAME (Continued)

Signal	LBD NO./Sources	Definition
TxWCM	5368Hx	Transport x, write permit
TxWEN	5372H5/H10 5372L5/L10	Transport x, write enable status
TxWRS	5368Hx	Transport x, write reset pulse
TxWST	5370Hx	Transport x, word strobe
VDCOO		Ground
VDCO6		-6 volts
W200K	5358F1	Write clock for 200 bpi density
W556K	5358G6	Write clock for 556 bpi density
W800K	5358B4	Write clock for 800 bpi density
WCCLK	5358H2	Write control clock
WCFMS	5358D5	Write control file-mark strobe
WCFOx	5358J4	Write control, frame rate counter bit x
WCFRK	5358L5	Write control frame rate clock
WCFSS	5358D6	Write control file strobe storage
WCNWS	5358C4	Write control normal write strobe
WCWFM	5358J10	Write control write file mark
WCWOX	5358E10	Write control, character counter bit x
WCWST	5358C9	Write control, character counter clock
WCWRP	5358G11	Write control, write reset pulse
WDATx	5354KX	Write data tracks 1 through 7
WDSTB	5354H7	Write control, data strobe to read/write register
WHOLD	5360C2	Write hold flip-flop
WOCPS	5360E8	Write control OCP storage
WRRES	5368F9	Write reset pulse
WRTDM	5360B4	Write control, write enable delay
WSCLK	5358G2	Write control, selected clock

TABLE II.- SIGNAL NAME (Concluded)

Signal	LBD No./Sources	Definition
WSTRB	5358L9	Write control, word strobe
XXXXx	5366EX	Selected transport address

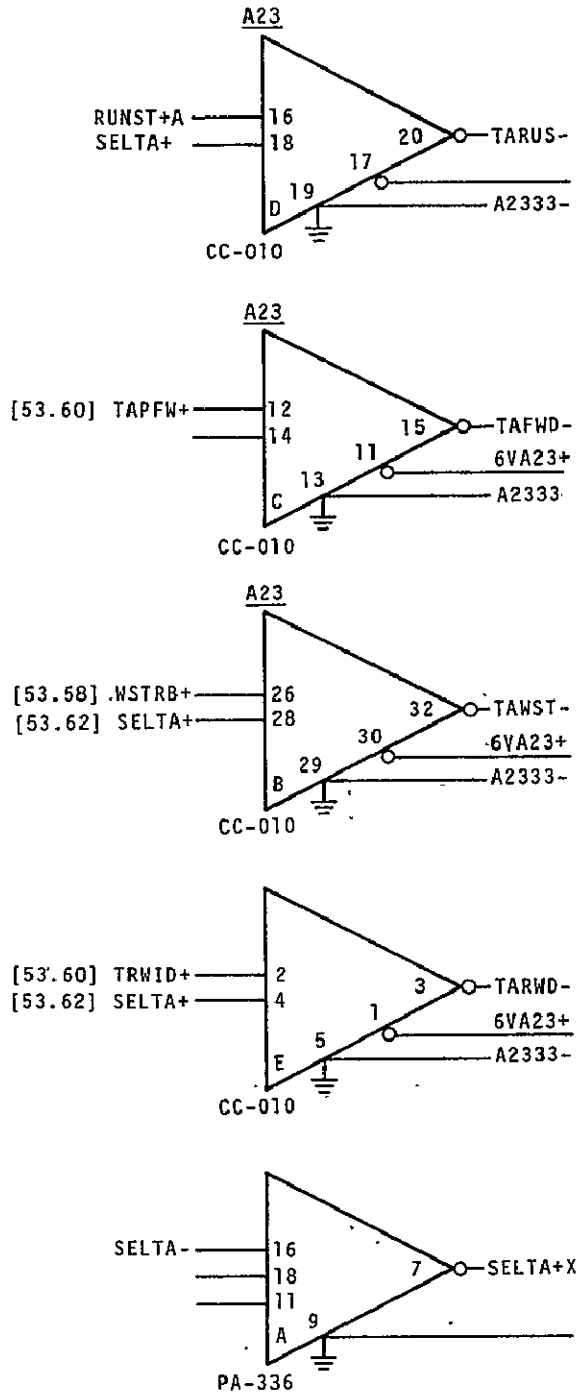


Figure 2-54. — Tape "A" driver logic (control bits).

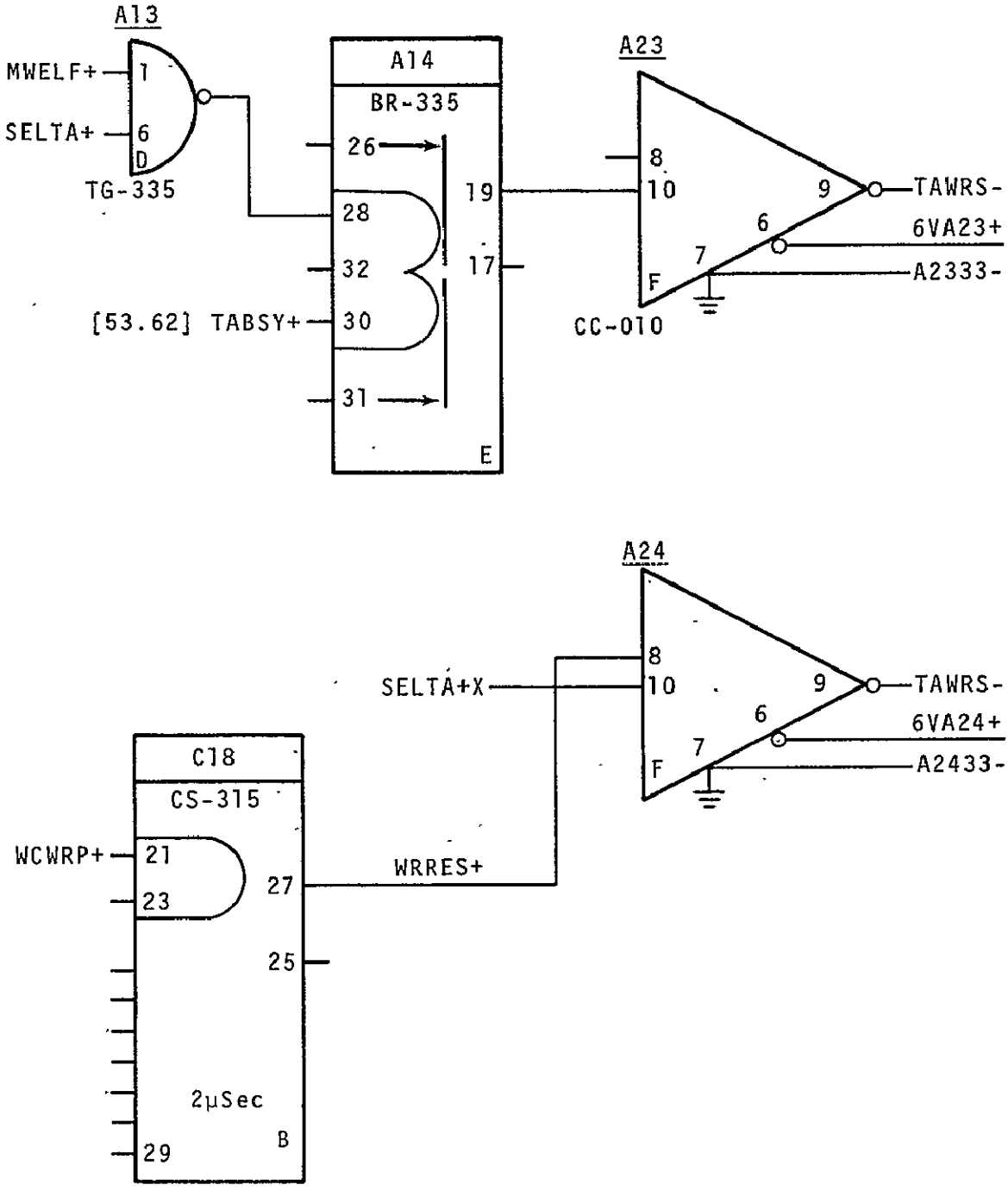


Figure 2-55. — Tape "A" driver logic (write command and write reset).

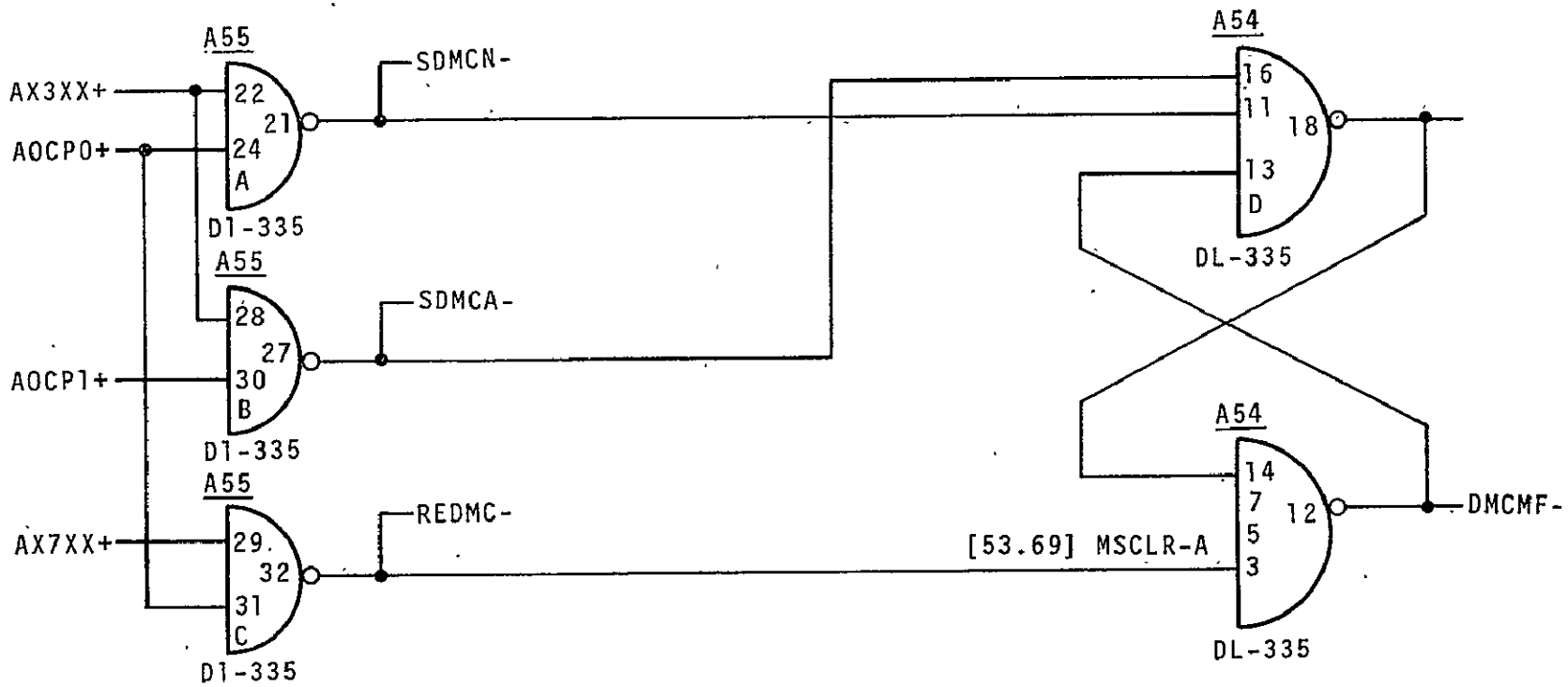


Figure 2-56.— DMC status latch.

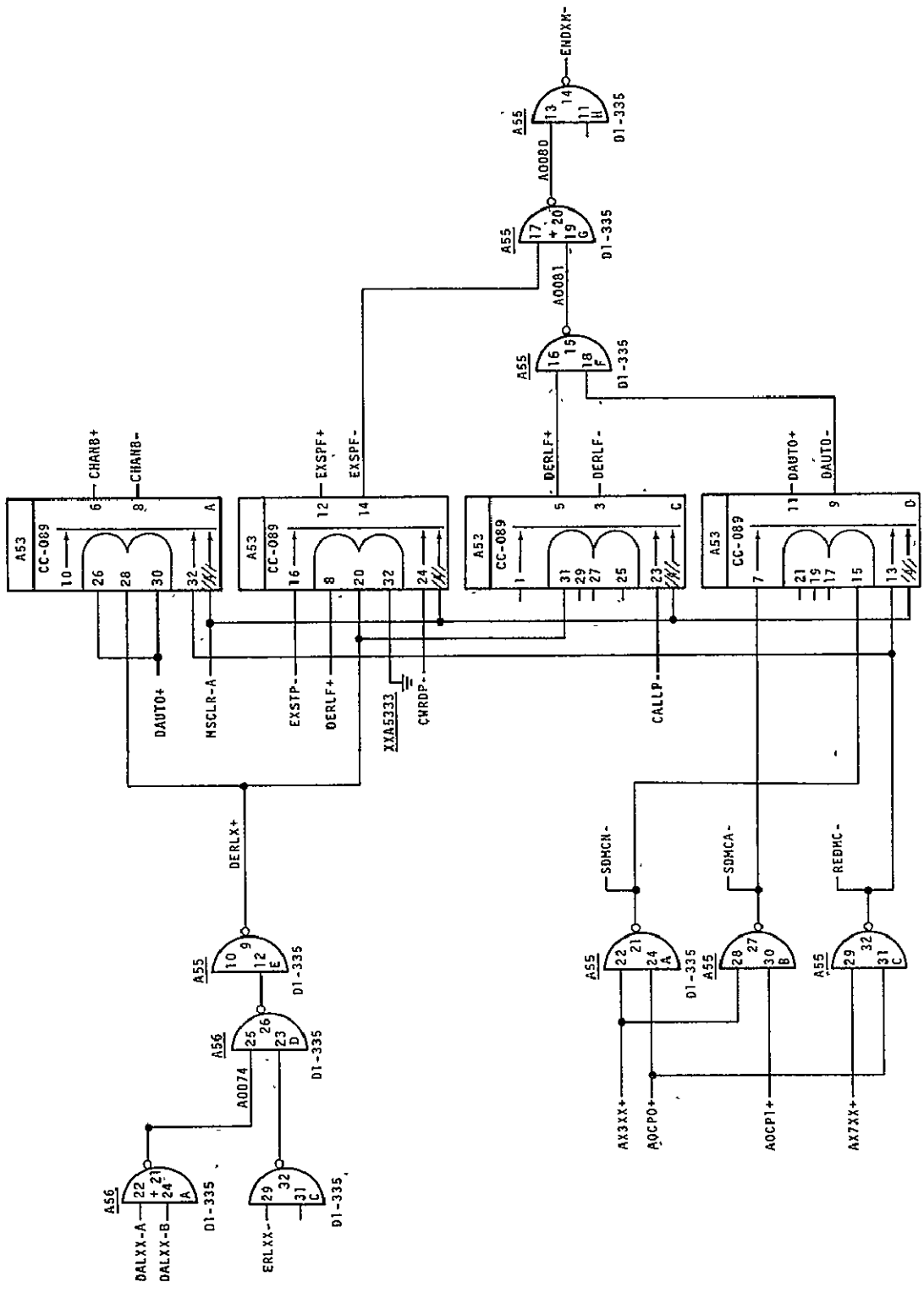


Figure 2-56. — DMC status latch.

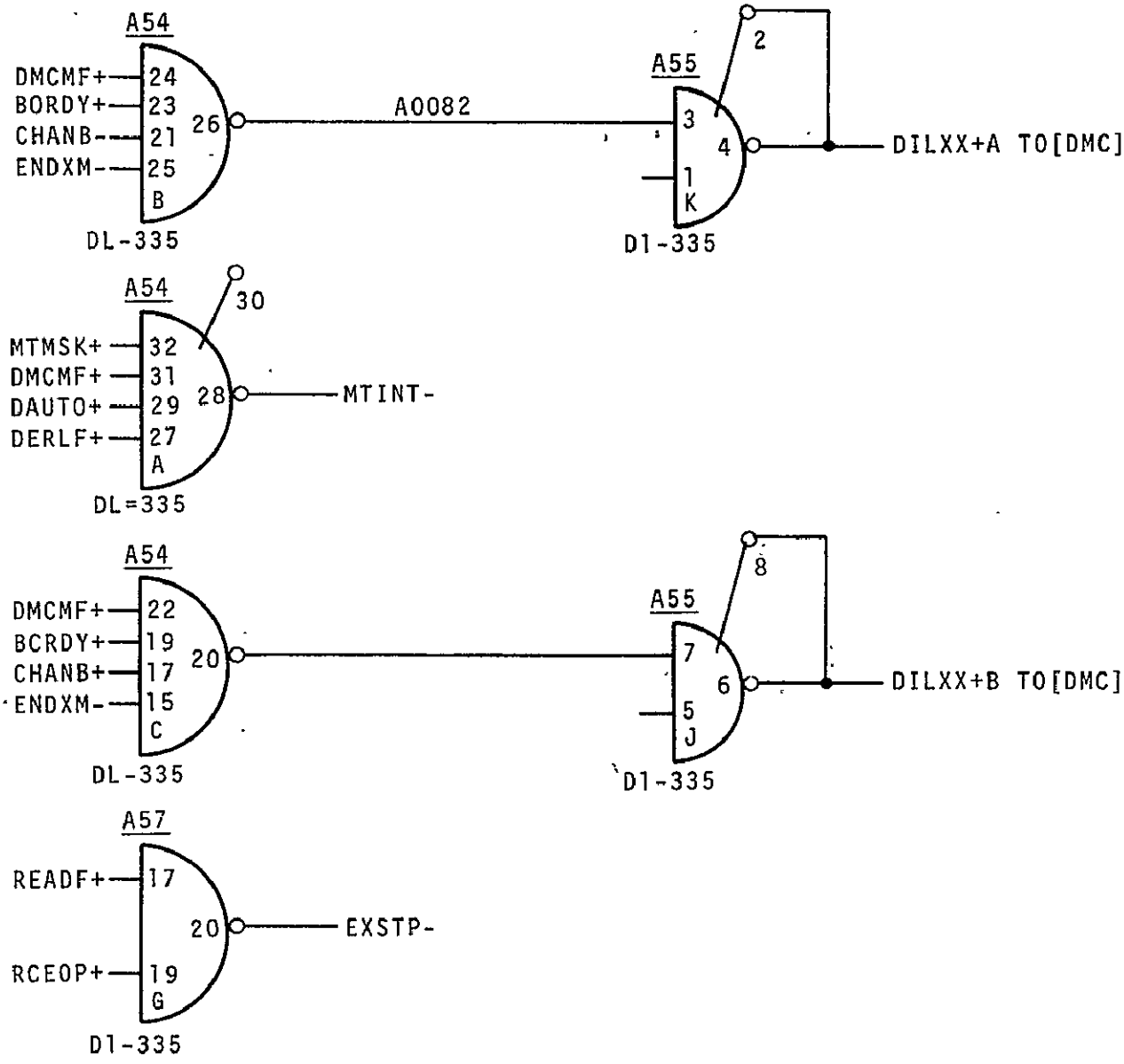


Figure 2-58.— DMC interrupt lines.

generates EXSPF- (external stop flip-flop) which will cause the end-of-transmission (ENDXM-) to be generated by gate A55H (figure 2-57). This signal is used to prevent further DMC interrupt by inhibiting gates A54B and A54C (figure 2-58).

During normal DMC write operations when the DMC reaches its end-of-range it transmits to the TCU an end-of-range signal (ERLXX) and this along with the correct device address line (DALXX) form the end-of-range signal (DERLX-). The gates which do this are shown in figure 2-59. Signal DERLX is used to set the end-of-range flip-flop A53C (figure 2-57) during normal operation. If the auto channel mode had been selected the auto switch flip-flop A53D (figure 2-57) would have inhibited the generation of the end-of-transmission signal ENDXM- (figure 2-57). If the auto mode had not been selected the external stop flip-flop A53B (figure 2-57) would have been set by DERLX+ which was generated by the DMC end-of-range signal ERLXX-).

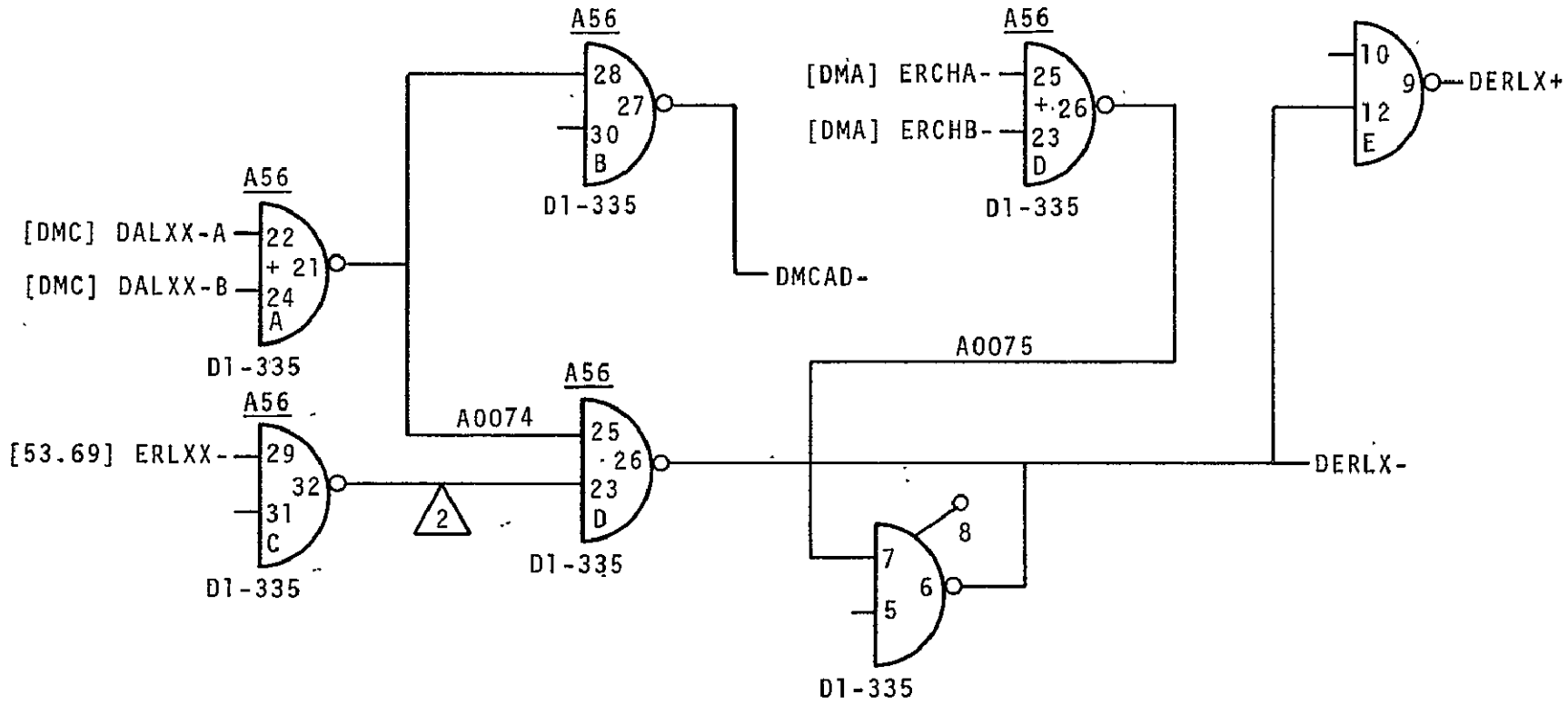


Figure 2-59. — DMC device address line and end-of-range.

3. PROGRAMMING REQUIREMENTS

3.1 STANDARD HONEYWELL DRIVER PROGRAMS

There are four programs required to operate the magnetic tape units. These are a read program, a write program, a control program, and a logical-to-physical tape unit number conversion program. The read program contains three parts which are called IØMA, IØMB, and IØMC.

These programs are used to read characters from the magnetic tape in one of three modes. IØMA reads two character BCD words even parity, IØMB reads two character binary words, odd parity, and IØMC reads three character binary words odd parity. The normal calling sequence used is as shown in figure 3-1. These three routines require 104_{10} storage locations.

The write program contains four parts which are called ØØMA, ØØMB, ØØMC, and ØØME. The first three routines, ØØMA, ØØMB, and ØØMC are the write routines required to write in the magnetic tape. ØØMA writes two characters per word BCD format, even parity; ØØMB writes two character per word binary format, odd parity; and ØØMC writes three characters per word binary format, odd parity. The calling sequence is shown in figure 3-2.

The routine ØØME is required to write an end-of-file mark on the tape. An end-of-file mark is an octal 17 and is used to block the tape off in large segments. The calling sequence is shown in figure 3-3. The routine MØUNIT is also required in any read or write sequence as will be shown in the MØUNIT discussion. The write routine requires 101_{10} storage locations.

The control program contains five parts which are called CØMR, CØFR, CØBR, CØFF, and CØBF. These routines are used to control tape search operations while looking for a particular record or file. CØMR is used to rewind the tape to the load point; CØFR is

```
CALL    IØMX    (Where X is A, B, or C)
DAC     BUFA    Buffer address
DEC     WC      Word count
DEC     N       Logical tape unit number
JMP     UNRE    Unreadable record return
JMP     EØT     End-of-tape return
JMP     EØF     End-of-file return
**              Normal return
```

Figure 3-1.— IØMX calling sequence.

```
CALL    ØØMX    (Where X is A, B, or C)
DAC     BUFA     Buffer address
DEC     WC       Word count
JMP     EØT      End-of-tape return
XX               Normal return
```

Figure 3-2.— ØØMX calling sequence.

```
CALL        ØSME        Call write file-mark
DEC         N           Logical tape unit number
**                      Normal return
```

Figure 3-3.— ØSME calling sequence.

C.2

used to space the tape forward one record; CØBR is used to space the tape back one record; CØFF is used to space the tape forward on file; and CØBF is used to space the tape back one file. The calling sequence for these five routines is shown in figure 3-4. The storage requirements for this routine is 67_{10} locations. The routine MØUNIT is also required for operation of this program.

The program MØUNIT is used to provide a physical tape unit number associated with a logical tape unit number when called by the read, write, or control routines. The physical tape unit number is any number between zero and 7 and the logical tape unit number is any number between 1 and 8. The logical tape unit number is converted to a physical number by means of a look-up table. Thus any physical tape unit number could be associated with any logical tape unit number.

MØUNIT also contains another look-up table for converting logical tape unit numbers to DMC channel numbers. This table is called MØCHAN and is accessed by way of a switch word called MØTY. If MØTY is a zero the program will return with a normal I/O device code but if MØTY is 1 the program will return with a DMC channel number and the tape operation will be via the DMC.

Tape unit 2 has device code numbers 14_8, 15_8, 16_8, and 17_8 and DMC channel numbers 3 and 4. It is not capable of operating the one Ampex TM7211 tape unit but will operate either or both Ampex TMZ recorders that are now in the Flight Controls Laboratory.

```
CALL        C$xx        Where xx is MR, FF, or BF
DEC         N           Logical tape unit number
**                      Normal return

CALL        C$xx        Where xx is FR or BR
DEC         N           Logical tape unit number
JMP         EOF         End-of-file return
**                      Normal return
```

Figure 3-4.— C$xx calling sequence.

4. REFERENCES

1. "Honeywell Interface Manual." Doc. no. 130071624.
2. "Honeywell, Ampex Tape Control Unit." Doc. no. 130071645E.
3. "Honeywell Programmer Reference Manual." Doc. no. 130071585C.
4. "Honeywell Micropac Manual." Doc. no. 130071369F.